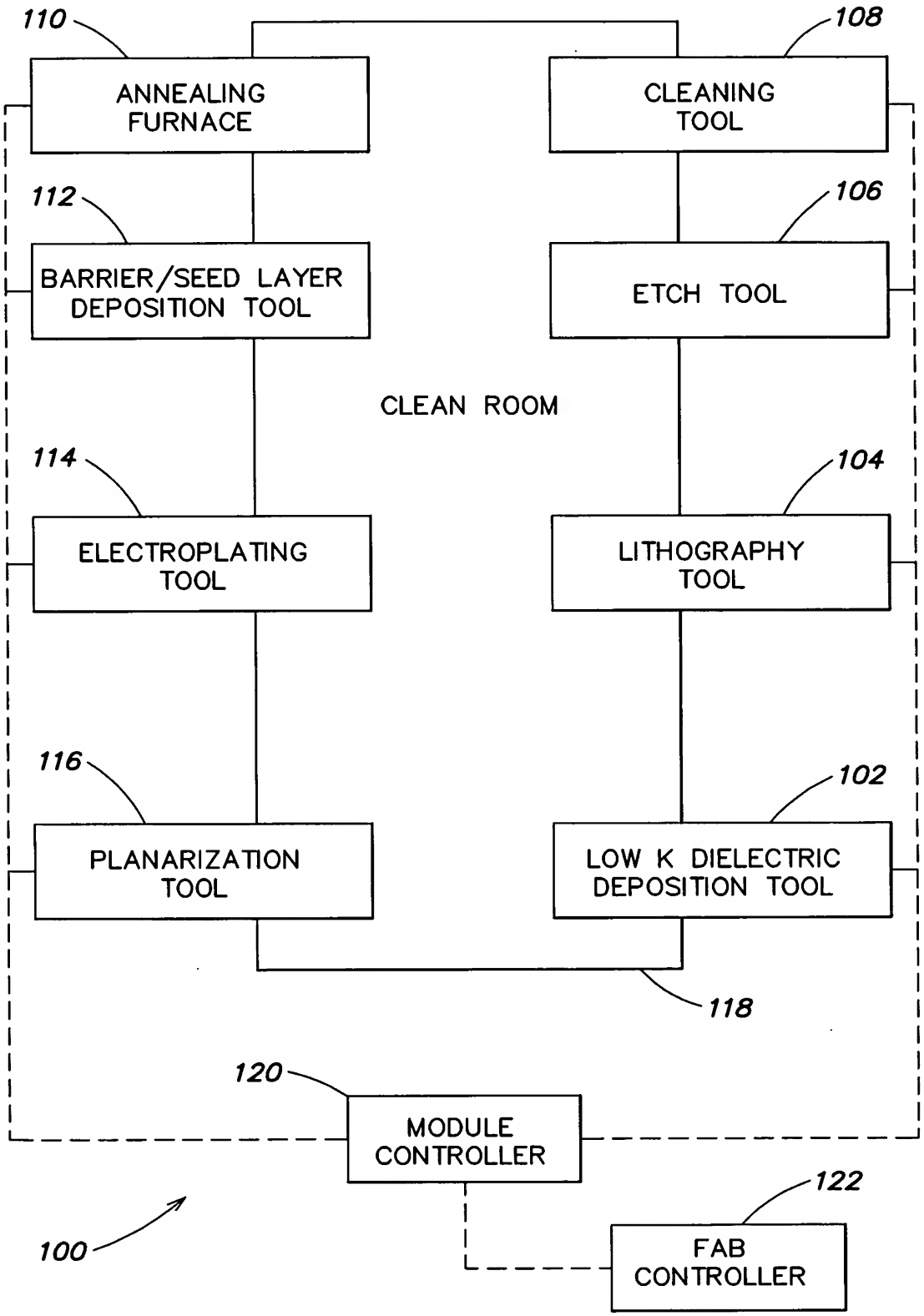

FIG. 1A

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
Filing Date: January 16, 2004

Express Mail Label No.: EV605116109US

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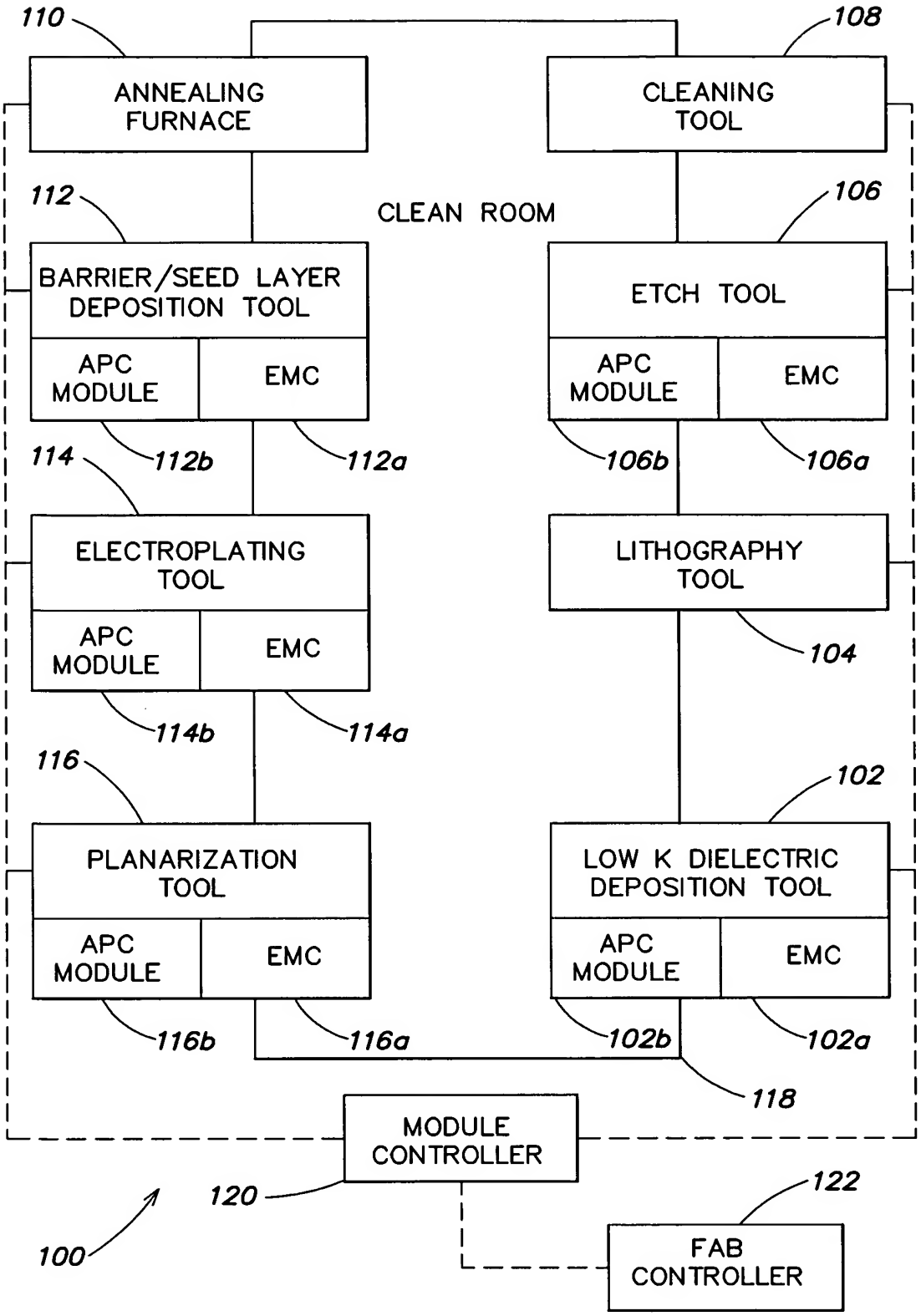
110
ANNEALING FURNACE
108
CLEANING TOOL
112
CLEAN ROOM
106
BARRIER/SEED LAYER DEPOSITION TOOL
APC MODULE
EMC
ETCH TOOL
APC MODULE
EMC
112b
112a
106b
106a
114
ELECTROPLATING TOOL
APC MODULE
EMC
LITHOGRAPHY TOOL
104
114b
114a
116
102
PLANARIZATION TOOL
APC MODULE
EMC
LOW K DIELECTRIC DEPOSITION TOOL
APC MODULE
EMC
116b
116a
102b
102a
118
MODULE CONTROLLER
120
122
FAB CONTROLLER
100

FIG. 1B

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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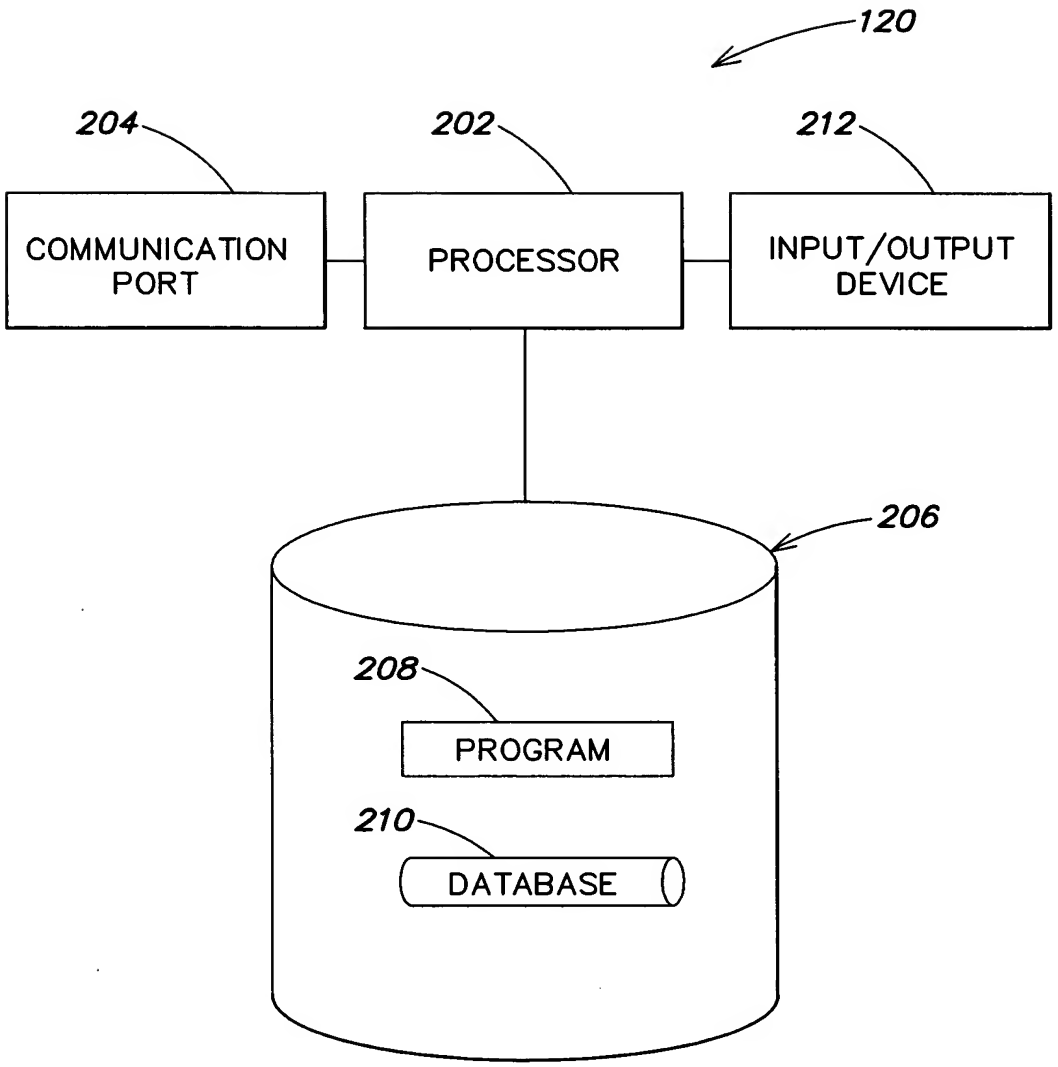
120
204
202
212
COMMUNICATION PORT
PROCESSOR
INPUT/OUTPUT DEVICE
206
208
PROGRAM
210
DATABASE

FIG. 2

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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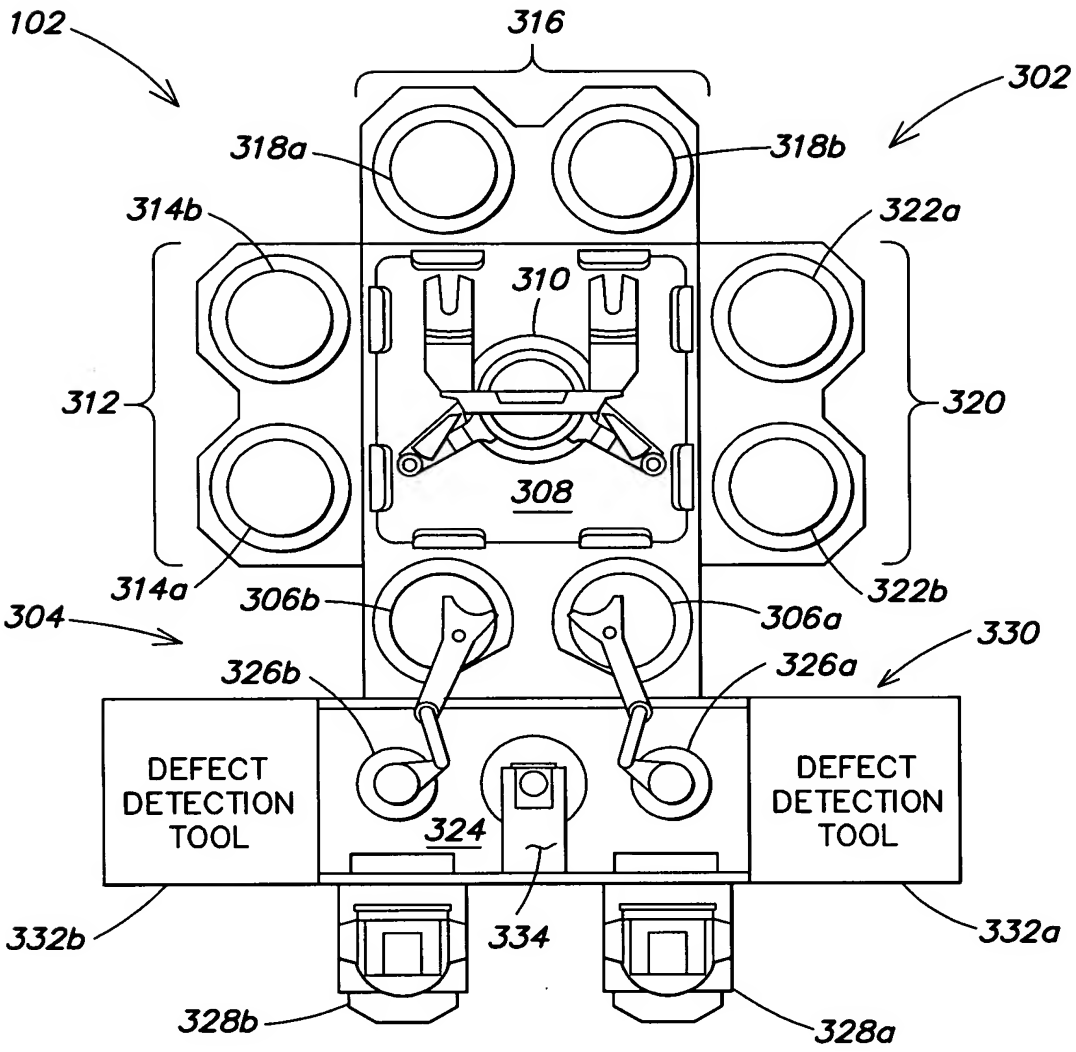
102
316
302
318a
318b
314b
322a
310
312
320
308
314a
322b
304
306b
306a
330
326b
326a
DEFECT DETECTION TOOL
DEFECT DETECTION TOOL
324
332b
334
332a
328b
328a

FIG. 3

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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Brian M. Dugan
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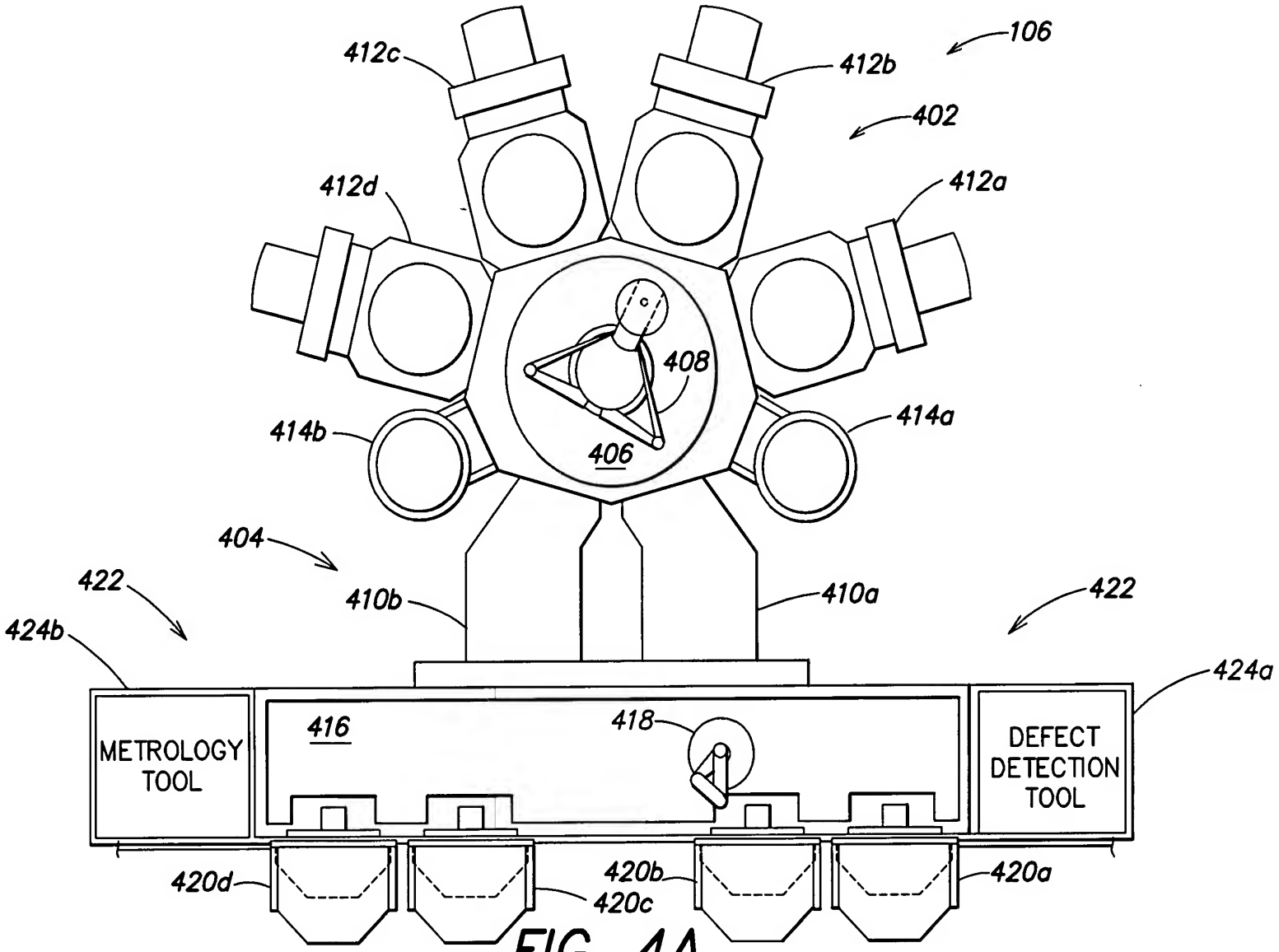
106
412c
412b
402
412d
412a
408
414b
414a
406
404
422
422
410b
410a
424b
424a
METROLOGY TOOL
416
418
DEFECT DETECTION TOOL
420d
420c
420b
420a

FIG. 4A

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
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Brian M. Dugan
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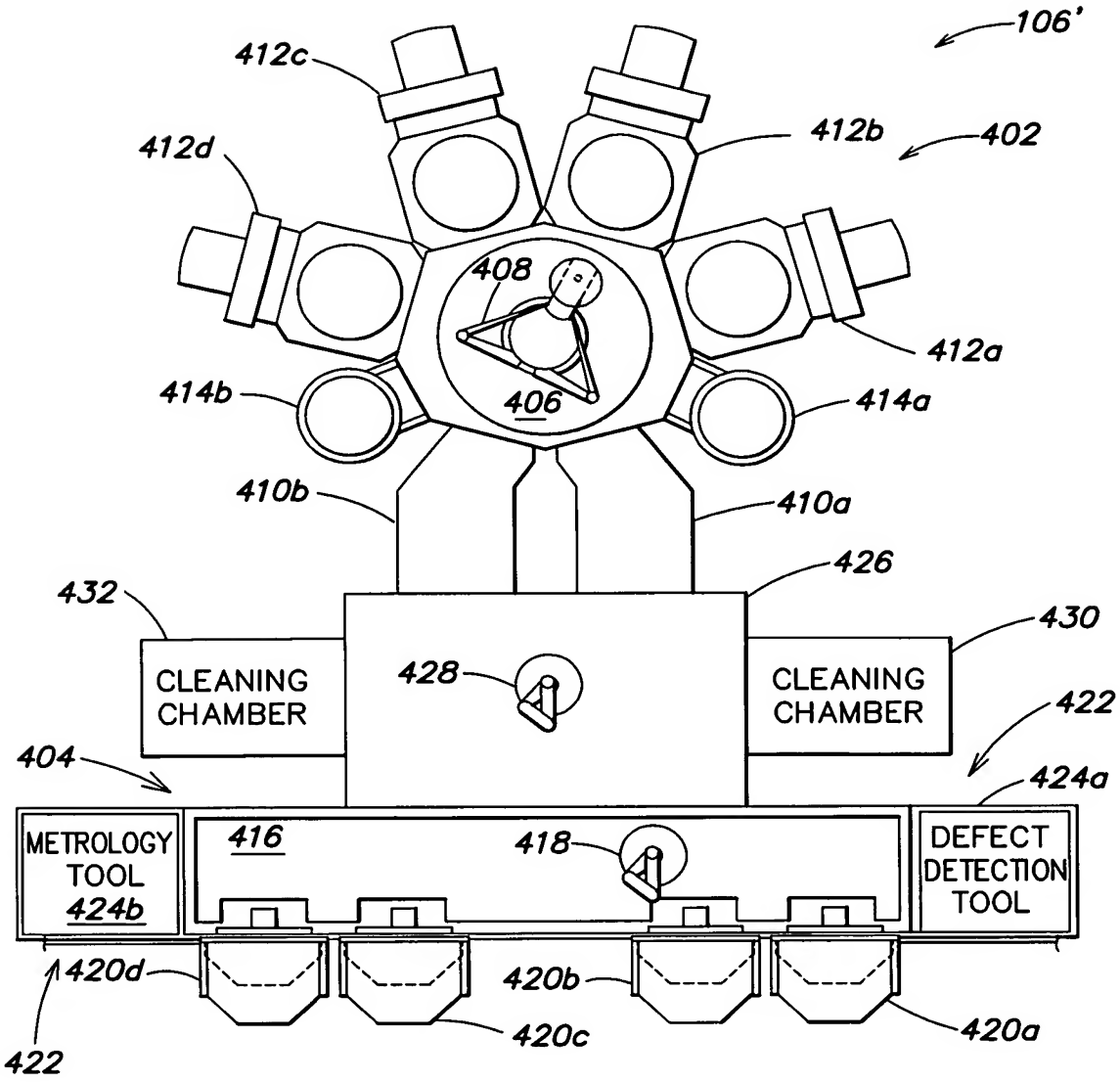
106'
412c
412b
402
412d
408
412a
414b
406
414a
410b
410a
426
432
430
CLEANING CHAMBER
428
CLEANING CHAMBER
422
404
424a
METROLOGY TOOL 424b
416
418
DEFECT DETECTION TOOL
420d
420b
420c
420a
422

FIG. 4B

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
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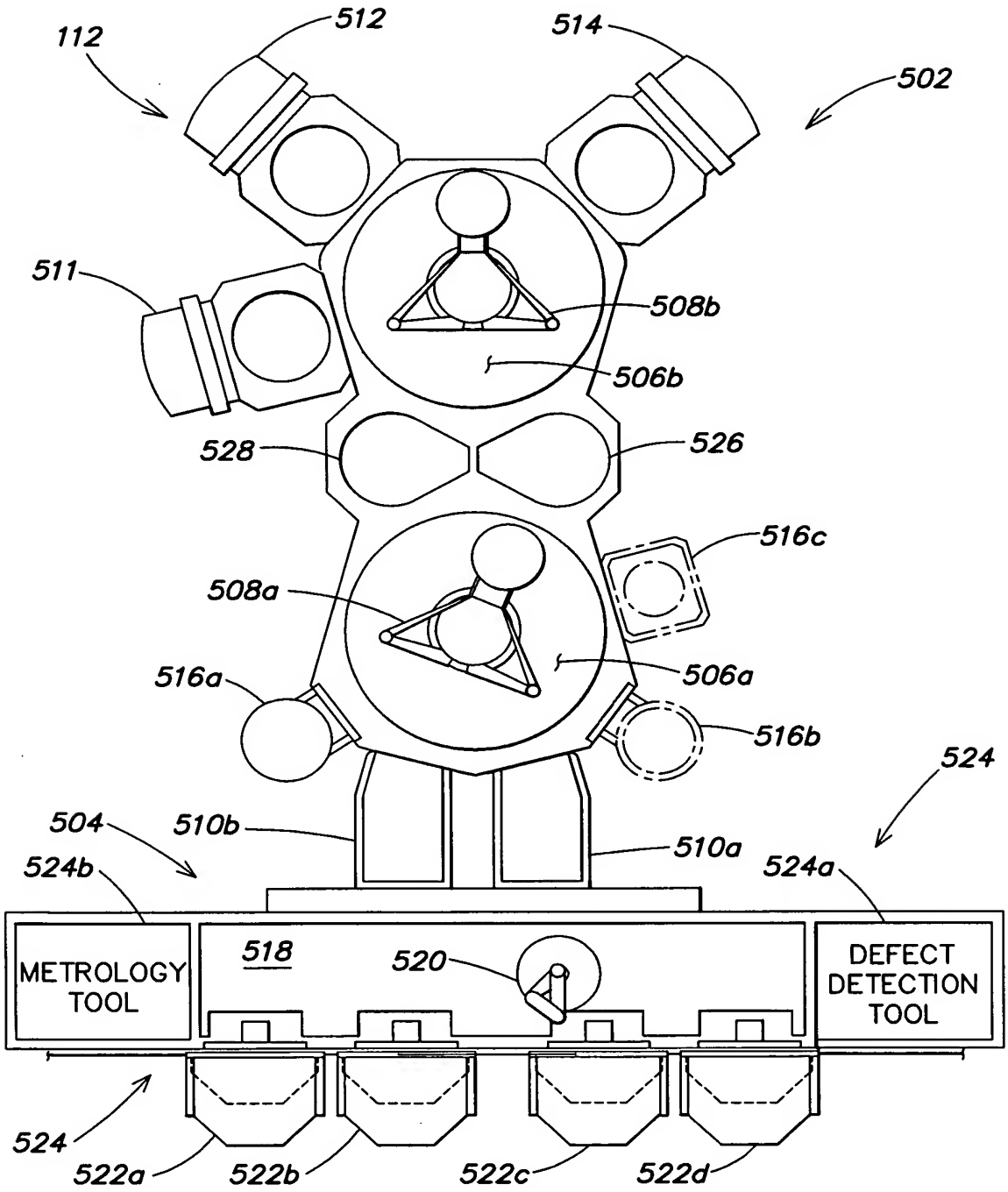
112
512
514
502
511
508b
506b
528
526
516c
508a
516a
506a
516b
524
504
510b
510a
524b
524a
METROLOGY TOOL
518
520
DEFECT DETECTION TOOL
524
522a
522b
522c
522d

FIG. 5

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
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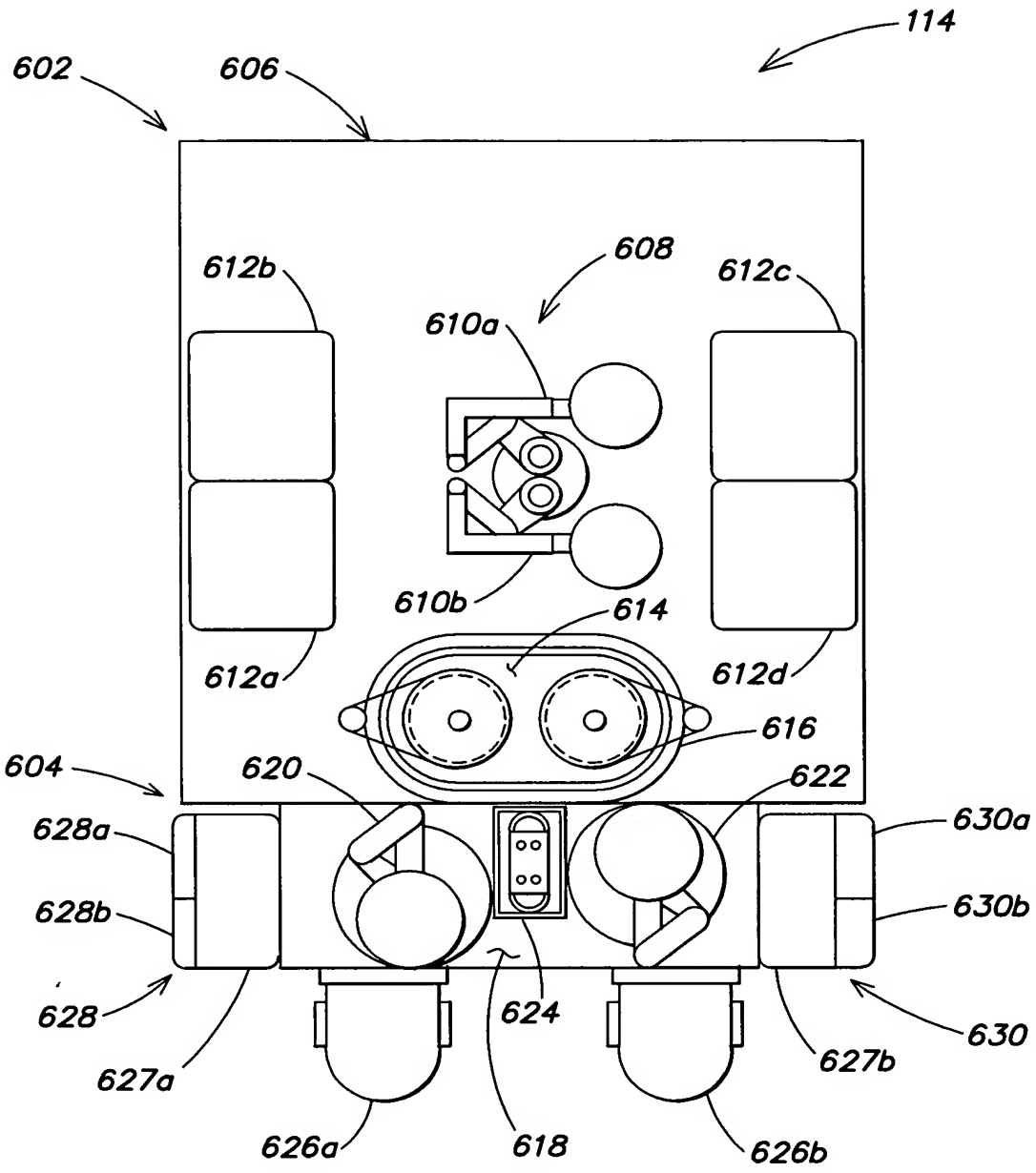
114
602
606
608
612b
612c
610a
610b
614
612a
612d
616
604
620
622
628a
630a
628b
630b
628
624
630
627a
627b
626a
618
626b

FIG. 6

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
Filing Date: January 16, 2004

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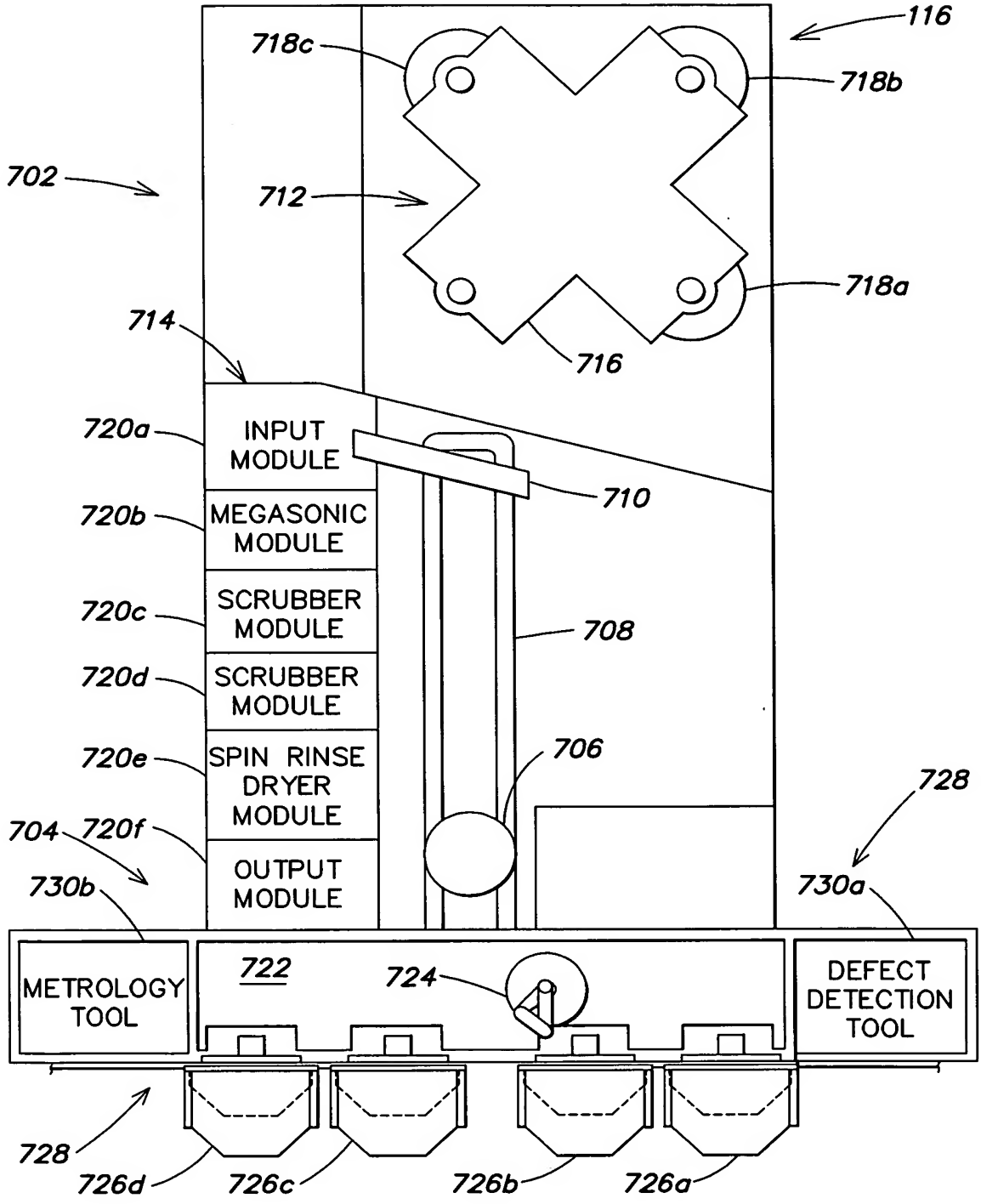
116
718c
718b
702
712
718a
714
716
720a
INPUT MODULE
710
720b
MEGASONIC MODULE
720c
SCRUBBER MODULE
708
720d
SCRUBBER MODULE
720e
SPIN RINSE DRYER MODULE
706
728
704
720f
OUTPUT MODULE
730b
730a
METROLOGY TOOL
722
724
DEFECT DETECTION TOOL
728
726d
726c
726b
726a

FIG. 7A

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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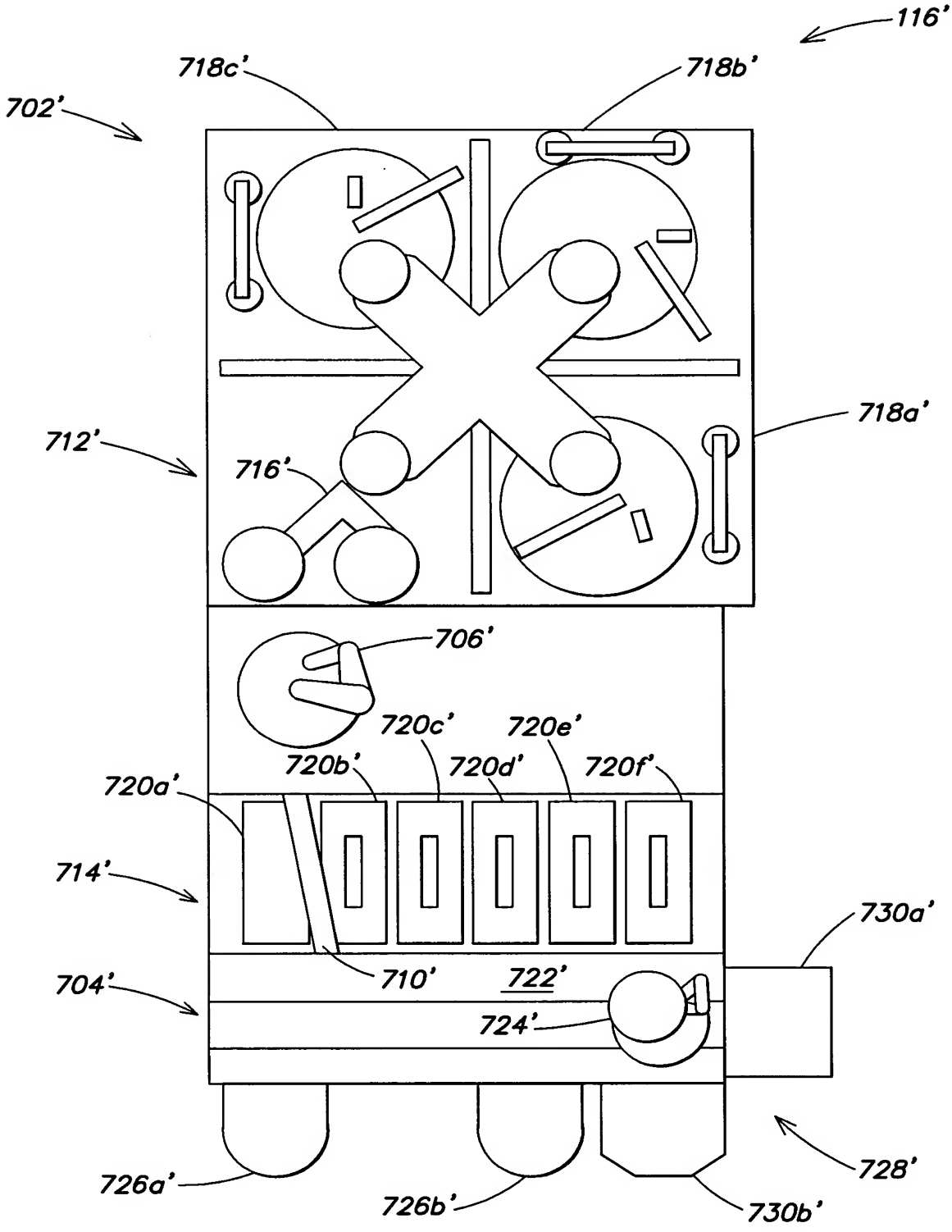
116'
718c'
718b'
702'
718a'
712'
716'
706'
720c'
720e'
720b'
720d'
720f'
720a'
714'
730a'
710'
722'
704'
724'
728'
726a'
726b'
730b'

FIG. 7B

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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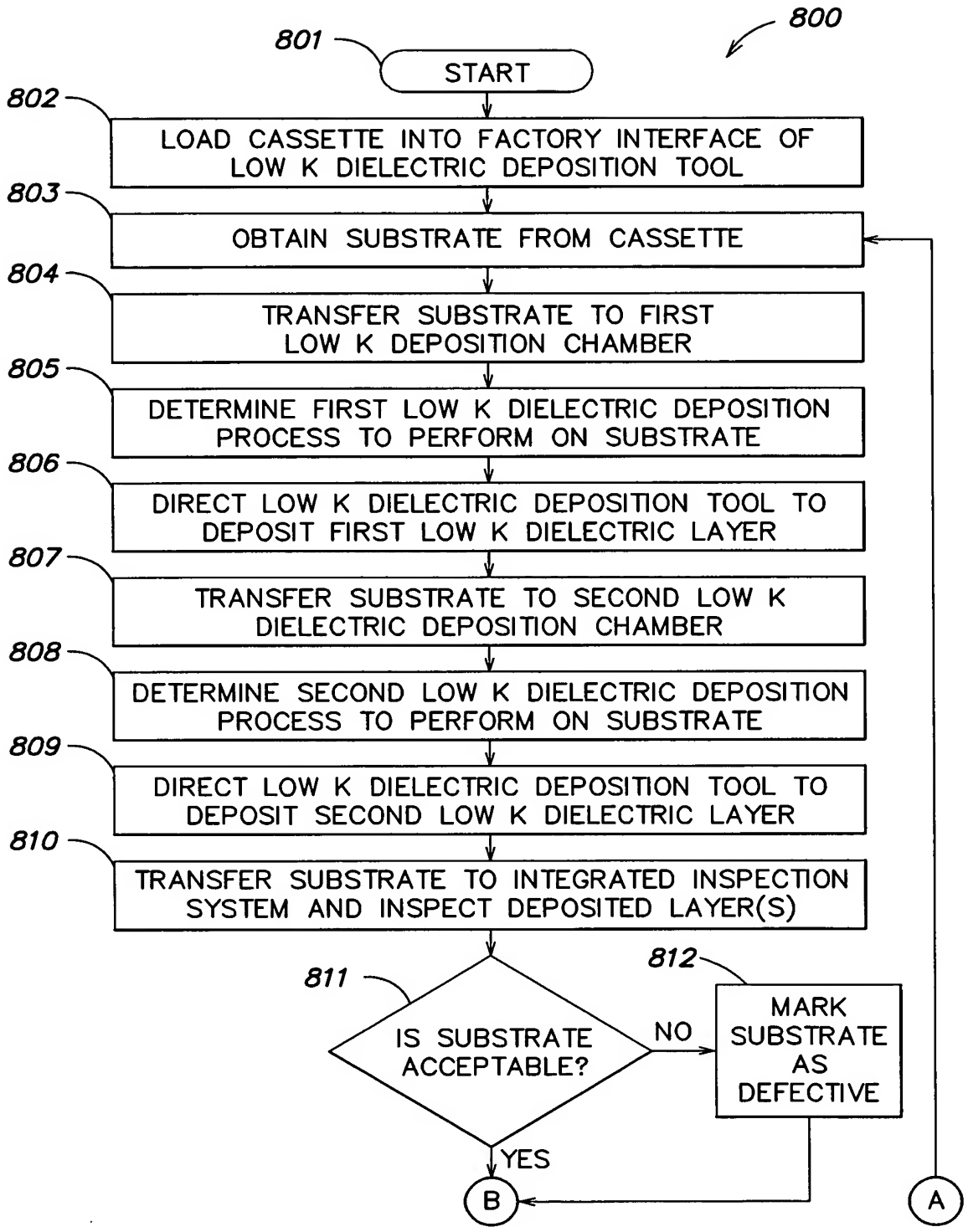
800
801
START
802
LOAD CASSETTE INTO FACTORY INTERFACE OF LOW K DIELECTRIC DEPOSITION TOOL
803
OBTAIN SUBSTRATE FROM CASSETTE
804
TRANSFER SUBSTRATE TO FIRST LOW K DEPOSITION CHAMBER
805
DETERMINE FIRST LOW K DIELECTRIC DEPOSITION PROCESS TO PERFORM ON SUBSTRATE
806
DIRECT LOW K DIELECTRIC DEPOSITION TOOL TO DEPOSIT FIRST LOW K DIELECTRIC LAYER
807
TRANSFER SUBSTRATE TO SECOND LOW K DIELECTRIC DEPOSITION CHAMBER
808
DETERMINE SECOND LOW K DIELECTRIC DEPOSITION PROCESS TO PERFORM ON SUBSTRATE
809
DIRECT LOW K DIELECTRIC DEPOSITION TOOL TO DEPOSIT SECOND LOW K DIELECTRIC LAYER
810
TRANSFER SUBSTRATE TO INTEGRATED INSPECTION SYSTEM AND INSPECT DEPOSITED LAYER(S)
811
IS SUBSTRATE ACCEPTABLE?
NO
812
MARK SUBSTRATE AS DEFECTIVE
YES
B
A

FIG. 8A

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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Brian M. Dugan
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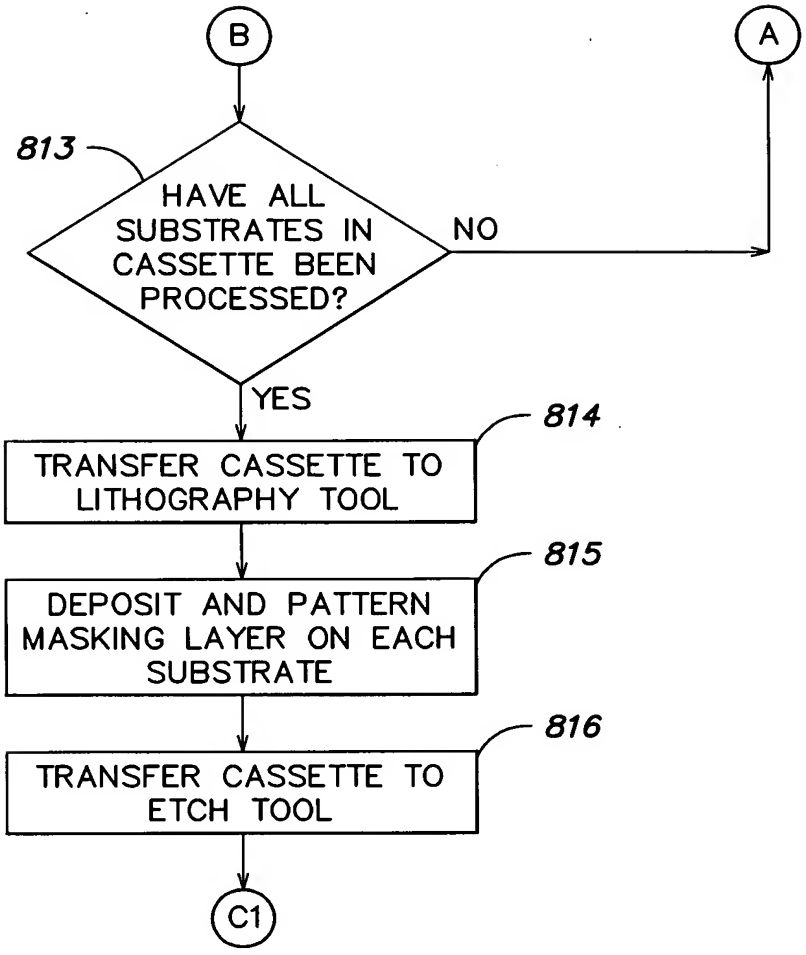
B
A
813
HAVE ALL SUBSTRATES IN CASSETTE BEEN PROCESSED?
NO
YES
814
TRANSFER CASSETTE TO LITHOGRAPHY TOOL
815
DEPOSIT AND PATTERN MASKING LAYER ON EACH SUBSTRATE
816
TRANSFER CASSETTE TO ETCH TOOL
C1

FIG. 8B

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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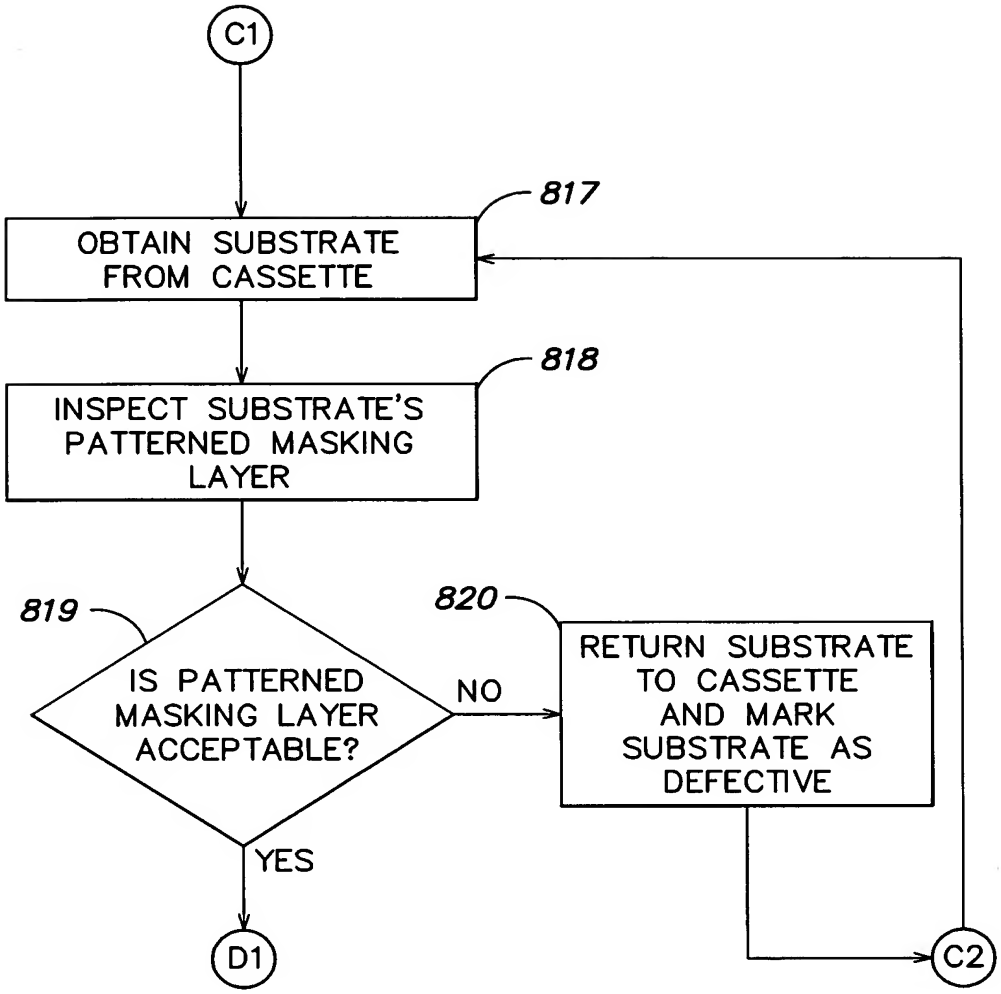
C1
817
OBTAIN SUBSTRATE FROM CASSETTE
818
INSPECT SUBSTRATE'S PATTERNED MASKING LAYER
819
IS PATTERNED MASKING LAYER ACCEPTABLE?
NO
820
RETURN SUBSTRATE TO CASSETTE AND MARK SUBSTRATE AS DEFECTIVE
YES
D1
C2

FIG. 8C

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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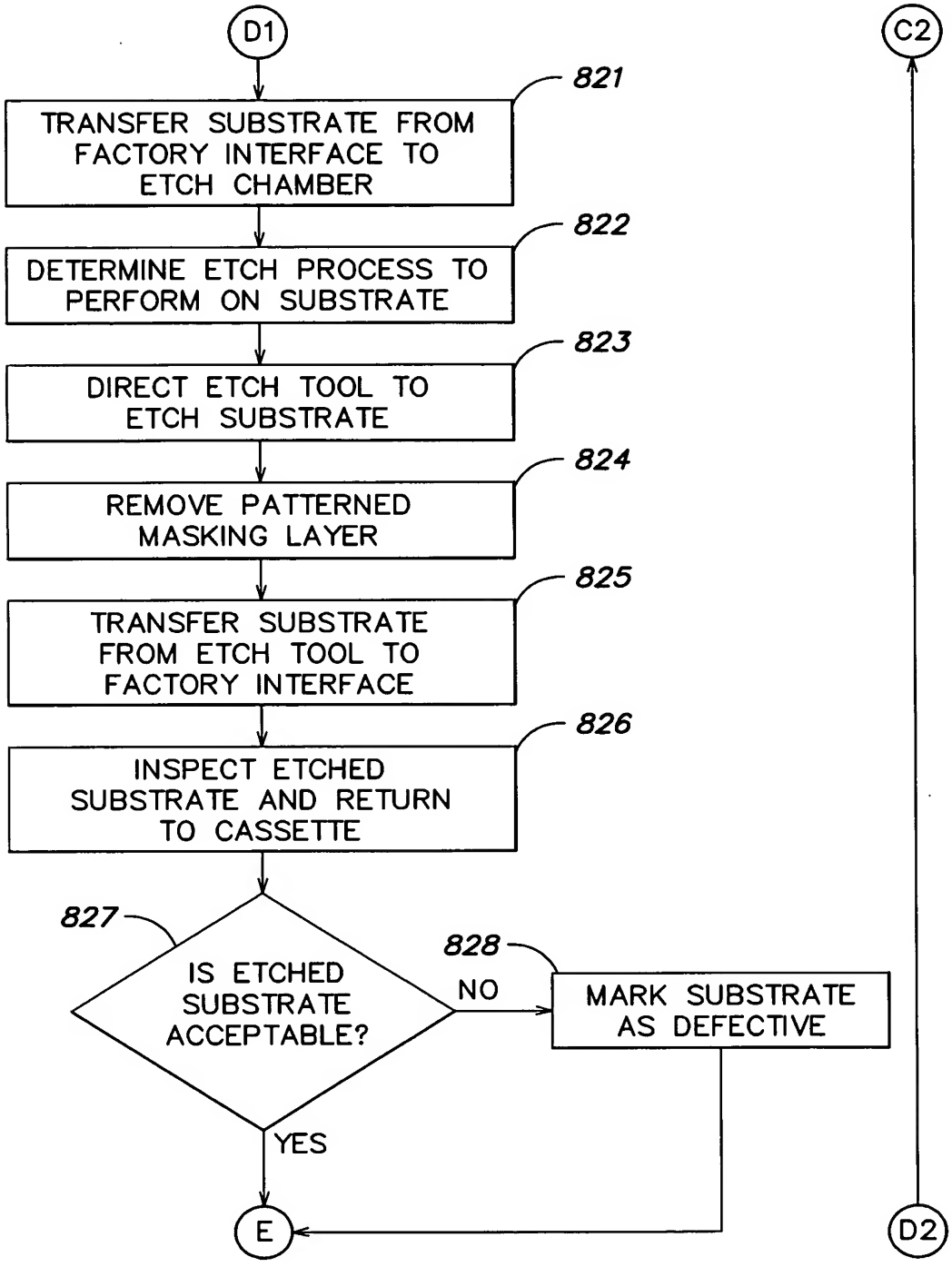
D1
C2
821
TRANSFER SUBSTRATE FROM FACTORY INTERFACE TO ETCH CHAMBER
822
DETERMINE ETCH PROCESS TO PERFORM ON SUBSTRATE
823
DIRECT ETCH TOOL TO ETCH SUBSTRATE
824
REMOVE PATTERNED MASKING LAYER
825
TRANSFER SUBSTRATE FROM ETCH TOOL TO FACTORY INTERFACE
826
INSPECT ETCHED SUBSTRATE AND RETURN TO CASSETTE
827
IS ETCHED SUBSTRATE ACCEPTABLE?
828
NO
MARK SUBSTRATE AS DEFECTIVE
YES
E
D2

FIG. 8D

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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Brian M. Dugan
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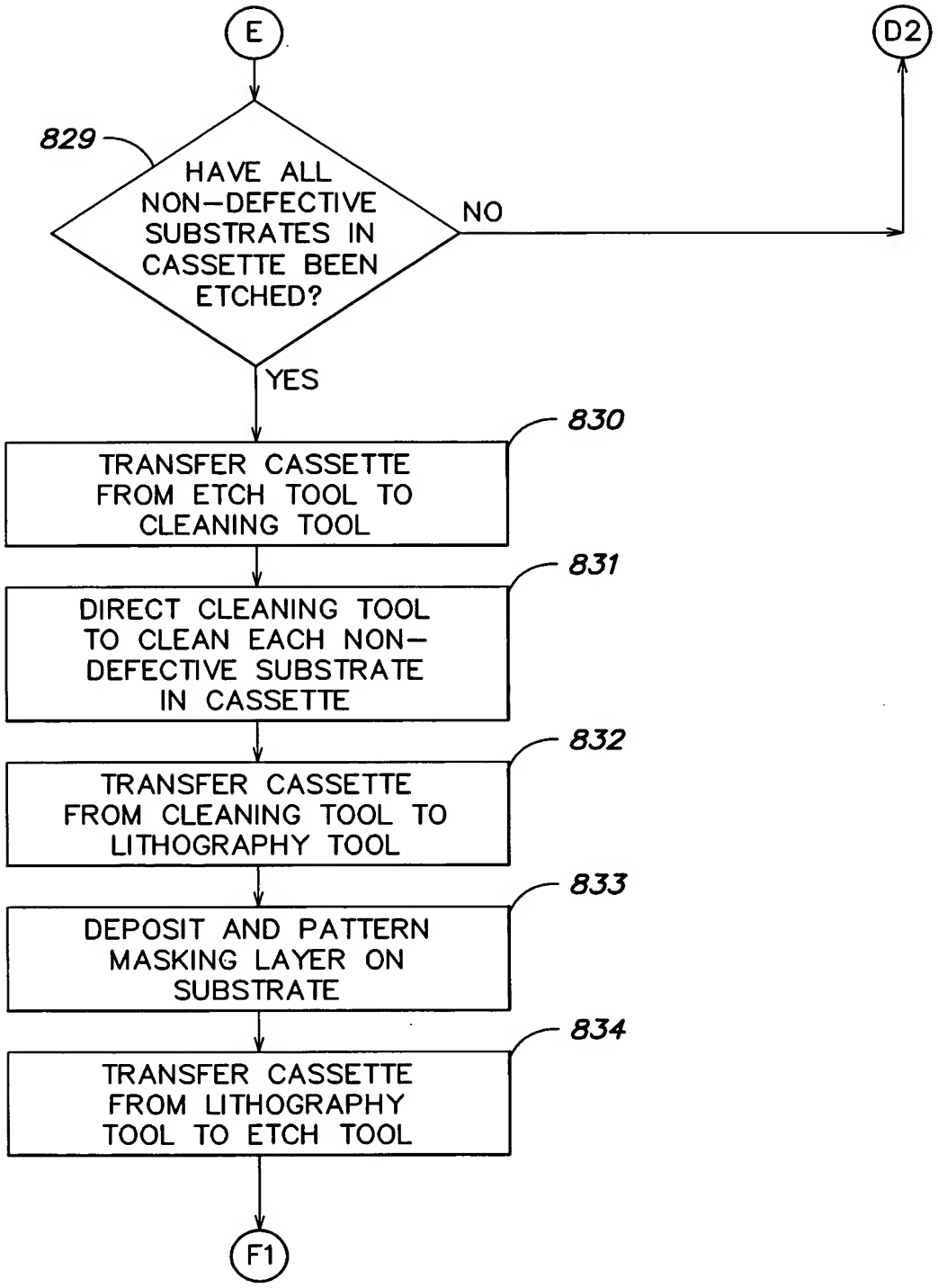
E
D2
829
HAVE ALL NON-DEFECTIVE SUBSTRATES IN CASSETTE BEEN ETCHED?
NO
YES
830
TRANSFER CASSETTE FROM ETCH TOOL TO CLEANING TOOL
831
DIRECT CLEANING TOOL TO CLEAN EACH NON-DEFECTIVE SUBSTRATE IN CASSETTE
832
TRANSFER CASSETTE FROM CLEANING TOOL TO LITHOGRAPHY TOOL
833
DEPOSIT AND PATTERN MASKING LAYER ON SUBSTRATE
834
TRANSFER CASSETTE FROM LITHOGRAPHY TOOL TO ETCH TOOL
F1

FIG. 8E

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
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Brian M. Dugan
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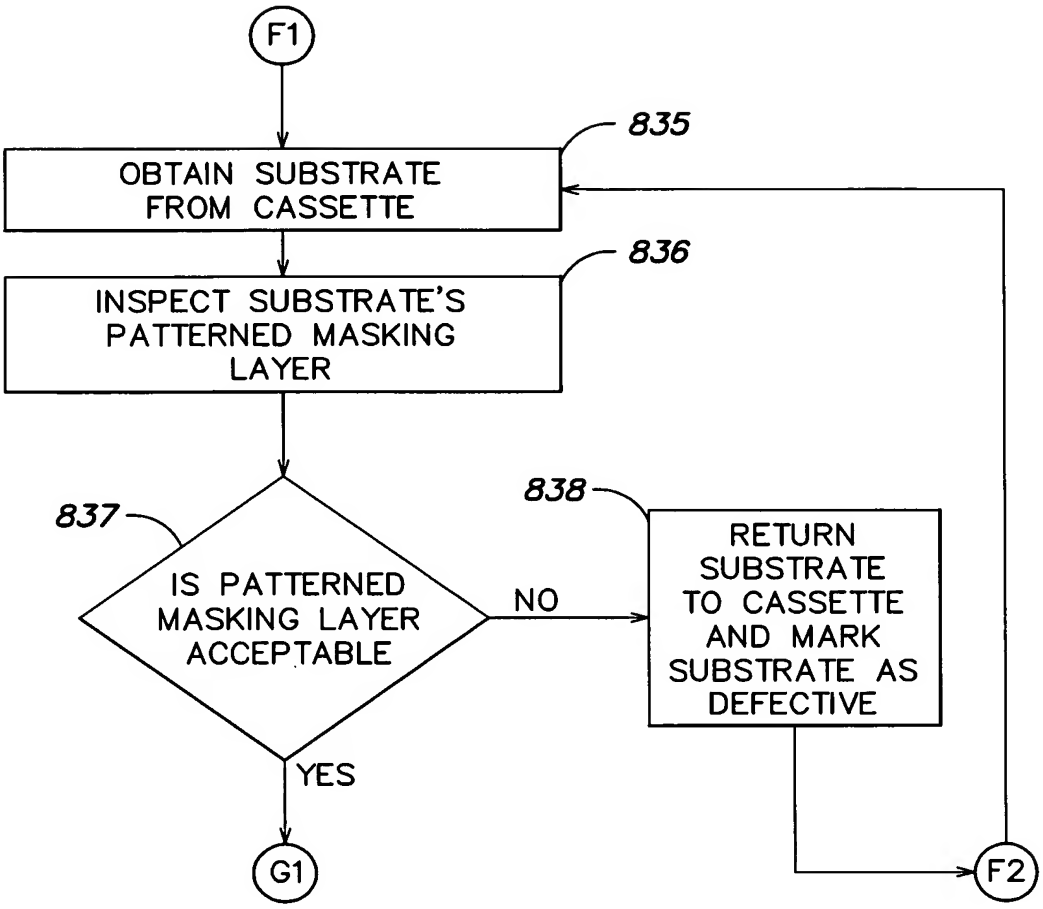
F1
835
OBTAIN SUBSTRATE FROM CASSETTE
836
INSPECT SUBSTRATE'S PATTERNED MASKING LAYER
837
IS PATTERNED MASKING LAYER ACCEPTABLE
NO
838
RETURN SUBSTRATE TO CASSETTE AND MARK SUBSTRATE AS DEFECTIVE
YES
G1
F2

FIG. 8F

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
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Brian M. Dugan
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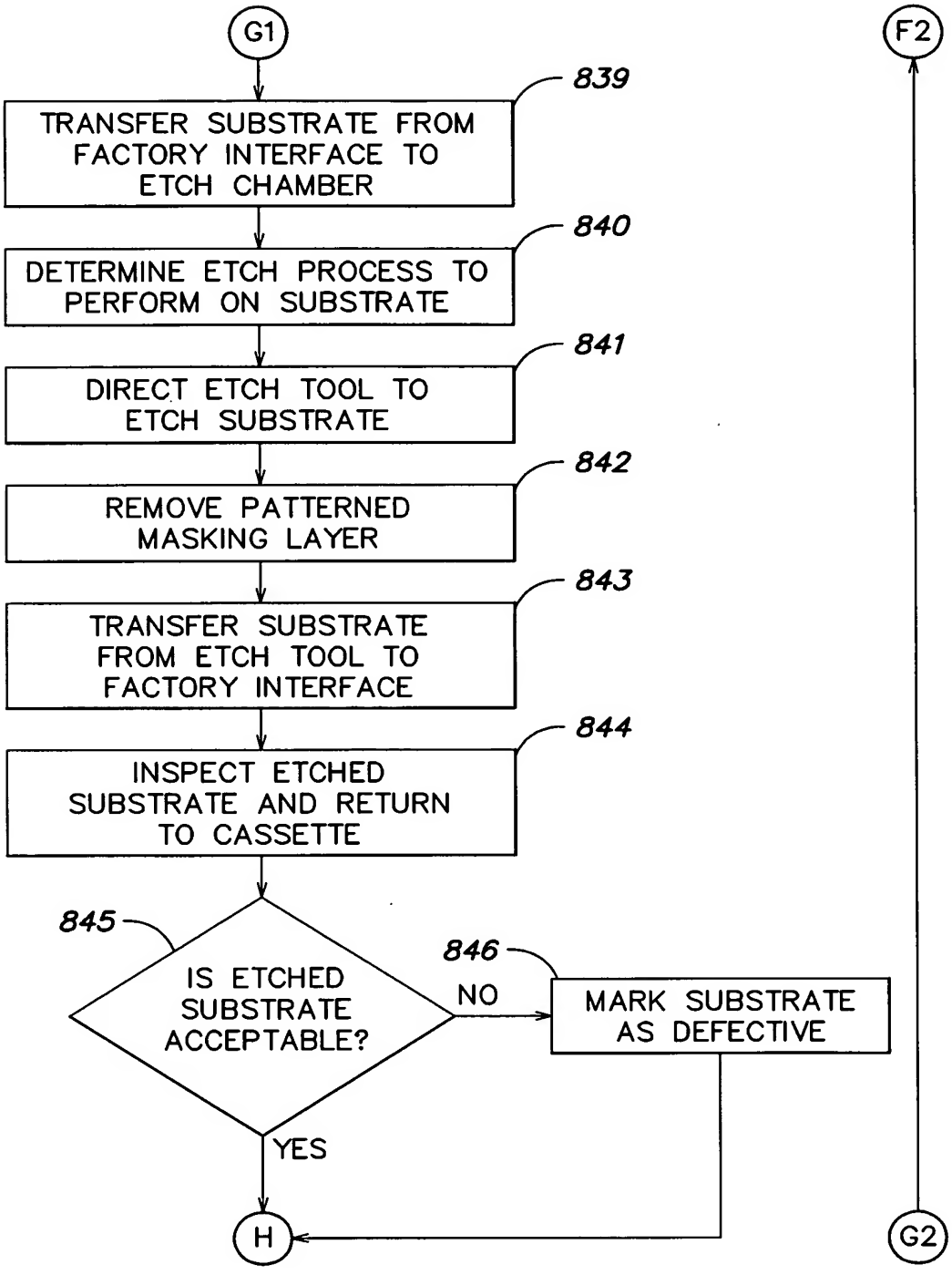
G1
F2
839
TRANSFER SUBSTRATE FROM FACTORY INTERFACE TO ETCH CHAMBER
840
DETERMINE ETCH PROCESS TO PERFORM ON SUBSTRATE
841
DIRECT ETCH TOOL TO ETCH SUBSTRATE
842
REMOVE PATTERNED MASKING LAYER
843
TRANSFER SUBSTRATE FROM ETCH TOOL TO FACTORY INTERFACE
844
INSPECT ETCHED SUBSTRATE AND RETURN TO CASSETTE
845
IS ETCHED SUBSTRATE ACCEPTABLE?
846
NO
MARK SUBSTRATE AS DEFECTIVE
YES
H
G2

FIG. 8G

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
Filing Date: January 16, 2004

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Brian M. Dugan
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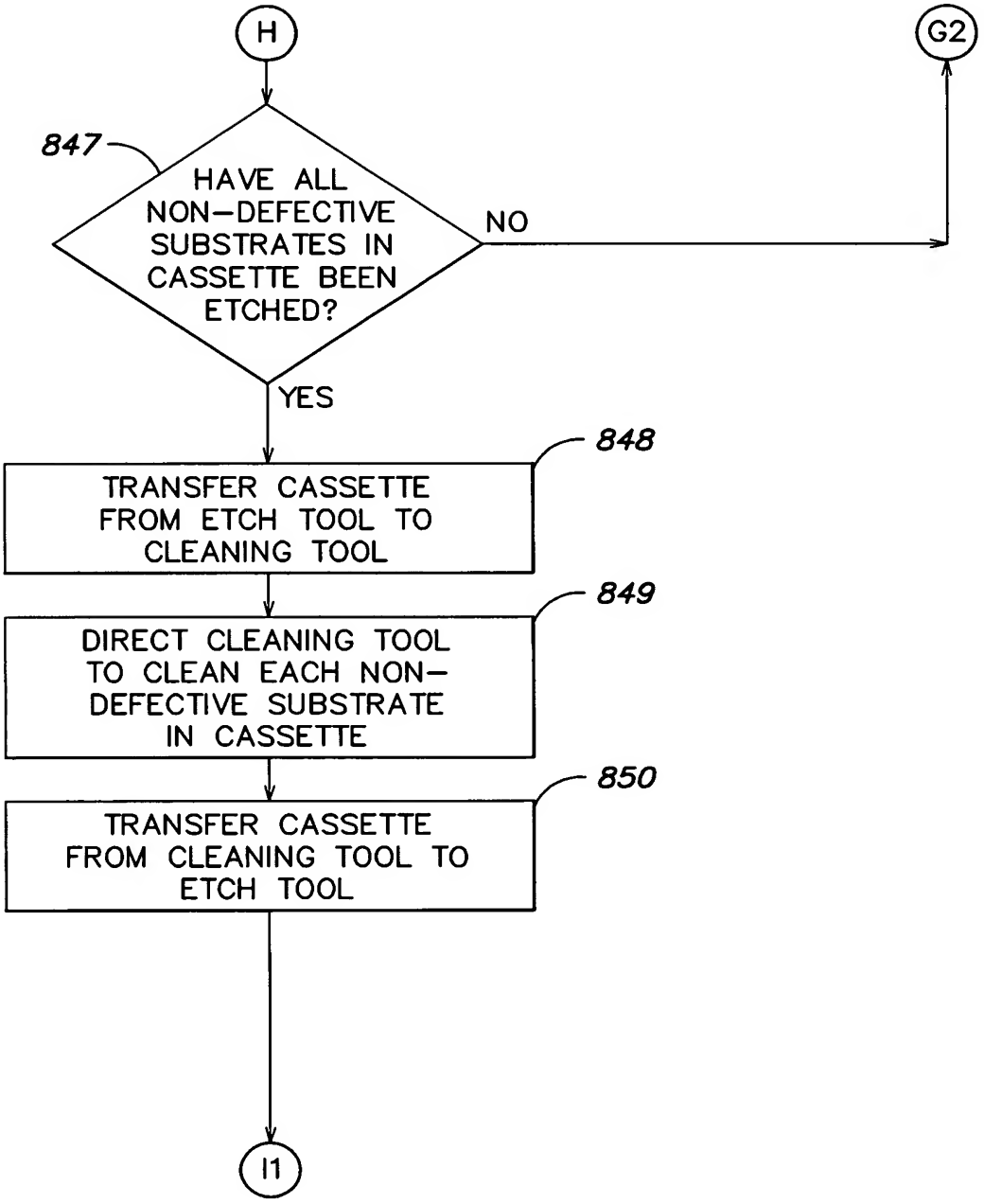
H
G2
847
HAVE ALL NON-DEFECTIVE SUBSTRATES IN CASSETTE BEEN ETCHED?
NO
YES
848
TRANSFER CASSETTE FROM ETCH TOOL TO CLEANING TOOL
849
DIRECT CLEANING TOOL TO CLEAN EACH NON-DEFECTIVE SUBSTRATE IN CASSETTE
850
TRANSFER CASSETTE FROM CLEANING TOOL TO ETCH TOOL
I1

FIG. 8H

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
Filing Date: January 16, 2004

Express Mail Label No.: EV605116109US

Brian M. Dugan
(914) 332-9081

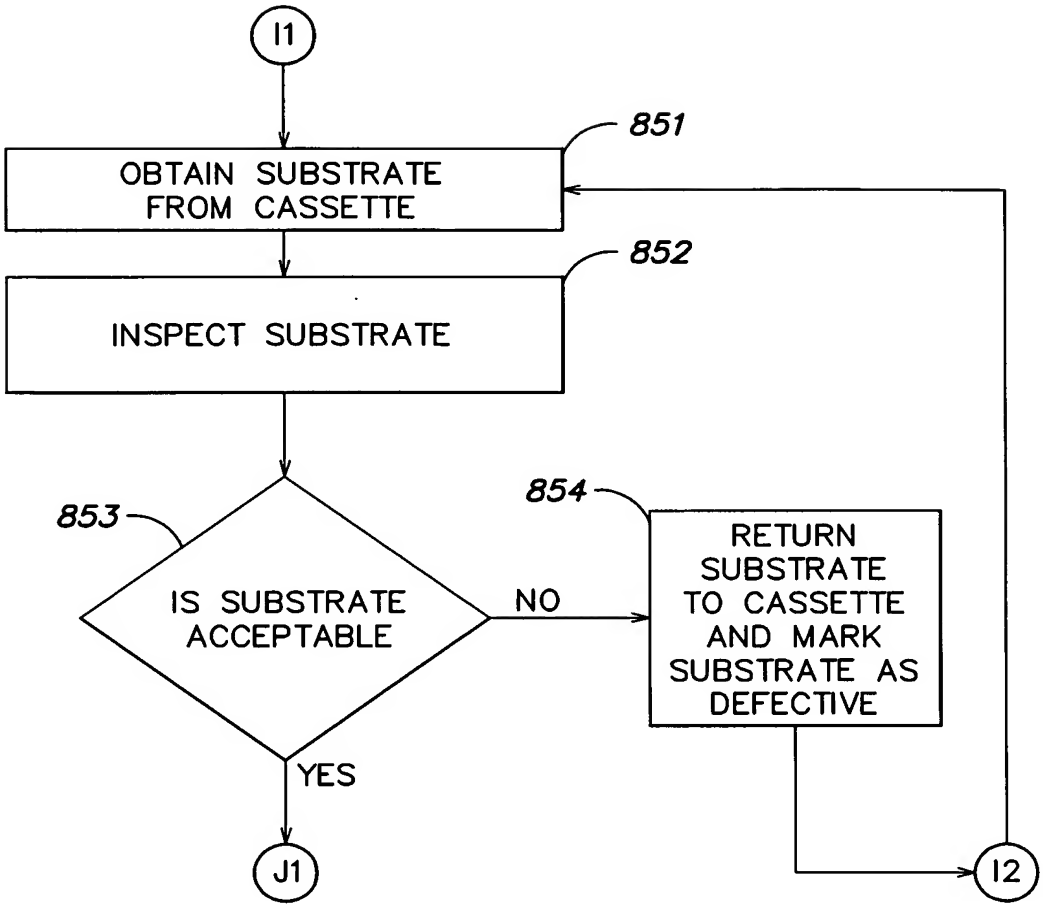
I1
851
OBTAIN SUBSTRATE FROM CASSETTE
852
INSPECT SUBSTRATE
853
IS SUBSTRATE ACCEPTABLE
NO
854
RETURN SUBSTRATE TO CASSETTE AND MARK SUBSTRATE AS DEFECTIVE
YES
J1
I2

FIG. 81

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
Filing Date: January 16, 2004

Express Mail Label No.: EV605116109US

Brian M. Dugan
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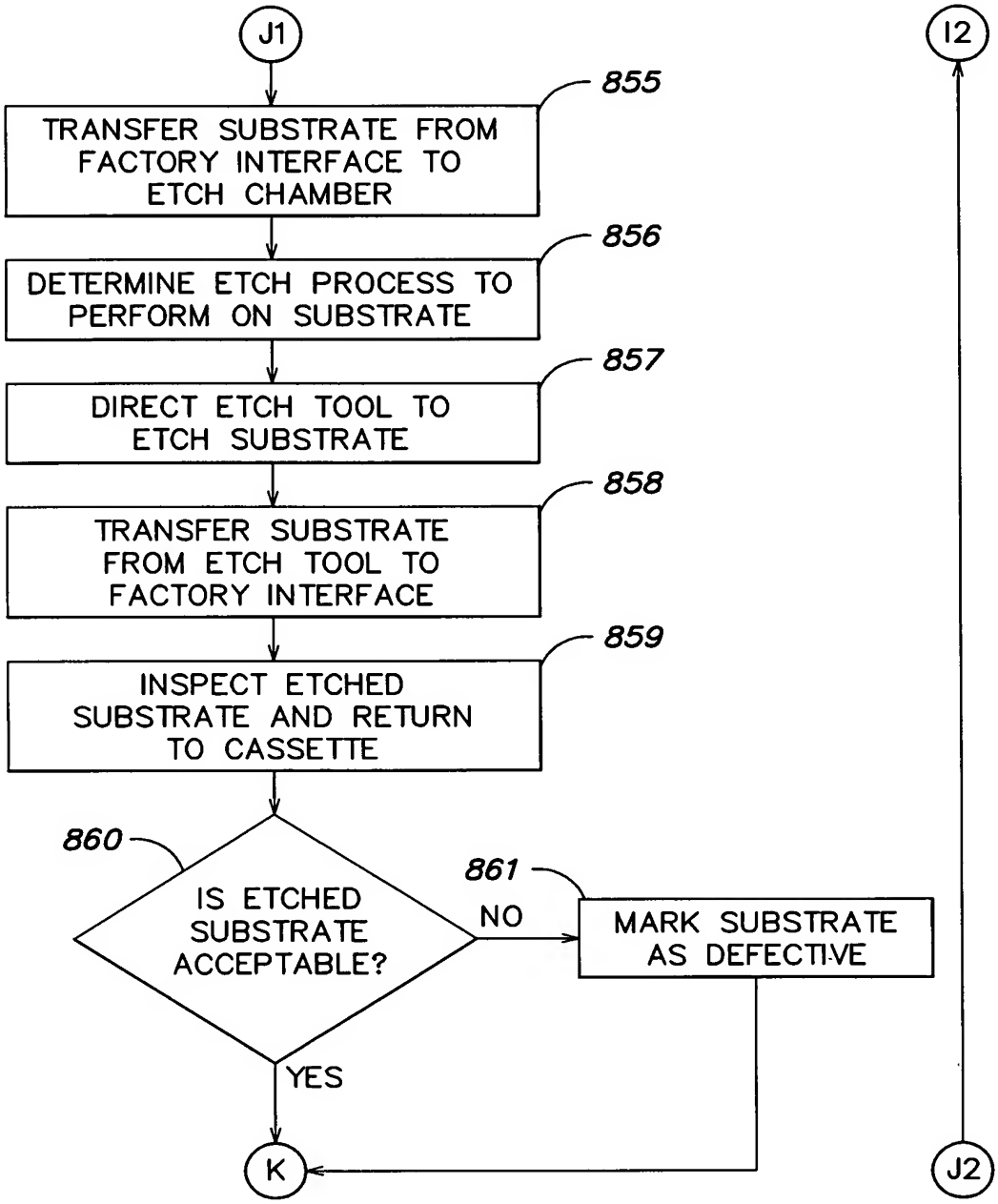
J1
855
TRANSFER SUBSTRATE FROM FACTORY INTERFACE TO ETCH CHAMBER
856
DETERMINE ETCH PROCESS TO PERFORM ON SUBSTRATE
857
DIRECT ETCH TOOL TO ETCH SUBSTRATE
858
TRANSFER SUBSTRATE FROM ETCH TOOL TO FACTORY INTERFACE
859
INSPECT ETCHED SUBSTRATE AND RETURN TO CASSETTE
860
IS ETCHED SUBSTRATE ACCEPTABLE?
861
NO
MARK SUBSTRATE AS DEFECTIVE
YES
K
I2
J2

FIG. 8J

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
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Brian M. Dugan
(914) 332-9081

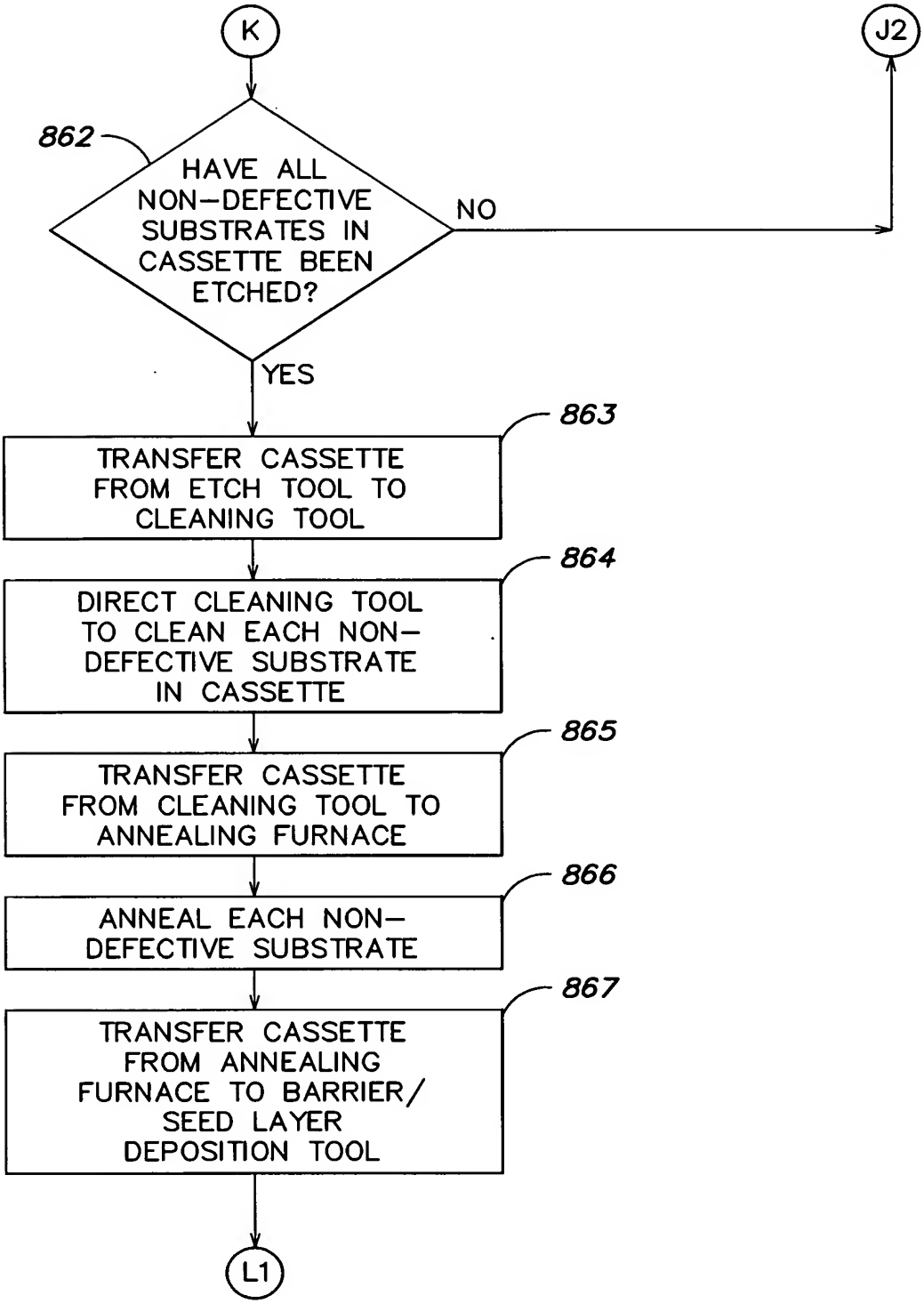
K
J2
862
HAVE ALL NON-DEFECTIVE SUBSTRATES IN CASSETTE BEEN ETCHED?
NO
YES
863
TRANSFER CASSETTE FROM ETCH TOOL TO CLEANING TOOL
864
DIRECT CLEANING TOOL TO CLEAN EACH NON-DEFECTIVE SUBSTRATE IN CASSETTE
865
TRANSFER CASSETTE FROM CLEANING TOOL TO ANNEALING FURNACE
866
ANNEAL EACH NON-DEFECTIVE SUBSTRATE
867
TRANSFER CASSETTE FROM ANNEALING FURNACE TO BARRIER/SEED LAYER DEPOSITION TOOL
L1

FIG. 8K

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
Filing Date: January 16, 2004

Express Mail Label No.: EV605116109US

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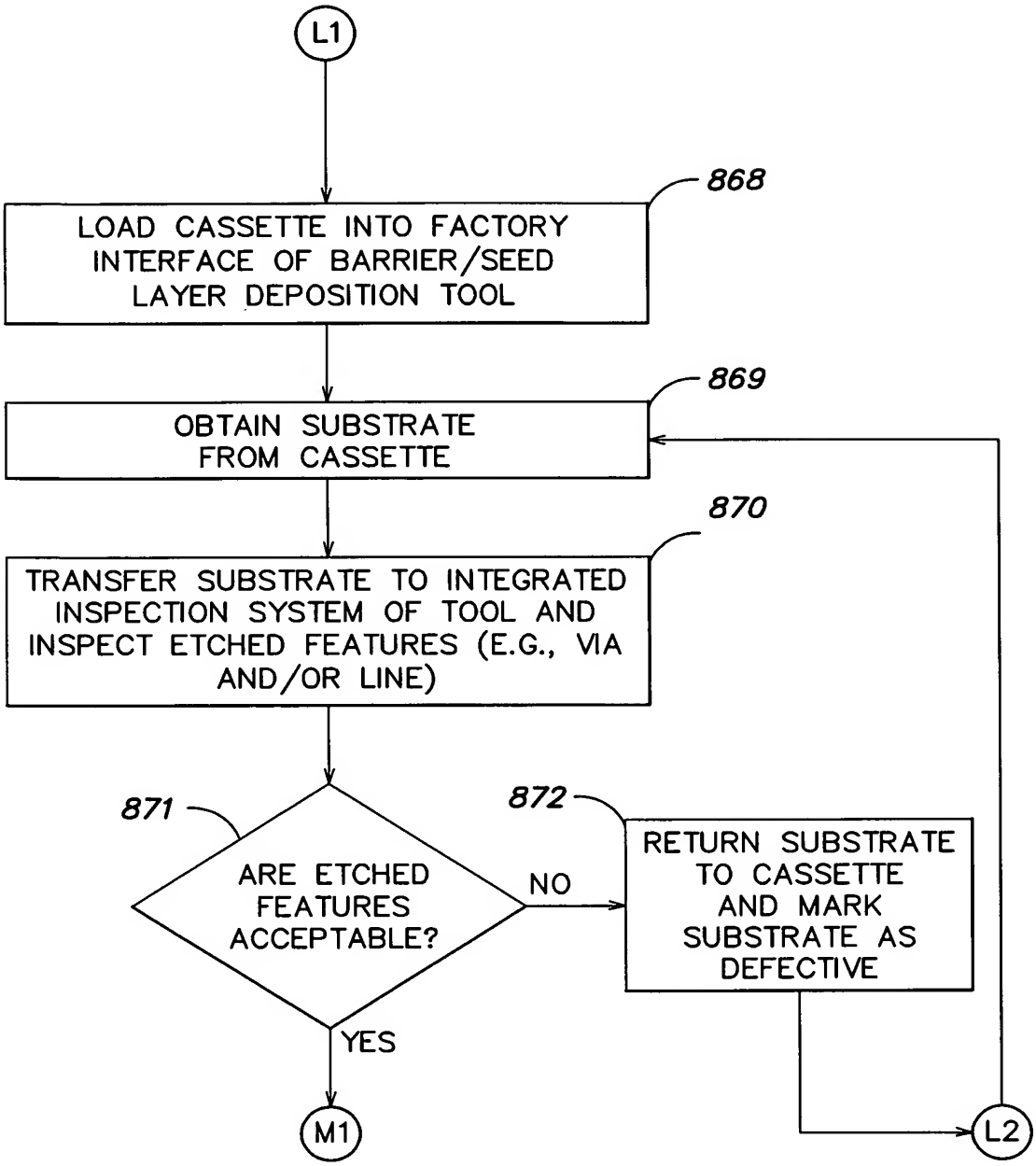
L1
868
LOAD CASSETTE INTO FACTORY INTERFACE OF BARRIER/SEED LAYER DEPOSITION TOOL
869
OBTAIN SUBSTRATE FROM CASSETTE
870
TRANSFER SUBSTRATE TO INTEGRATED INSPECTION SYSTEM OF TOOL AND INSPECT ETCHED FEATURES (E.G., VIA AND/OR LINE)
871
ARE ETCHED FEATURES ACCEPTABLE?
NO
872
RETURN SUBSTRATE TO CASSETTE AND MARK SUBSTRATE AS DEFECTIVE
YES
M1
L2

FIG. 8L

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
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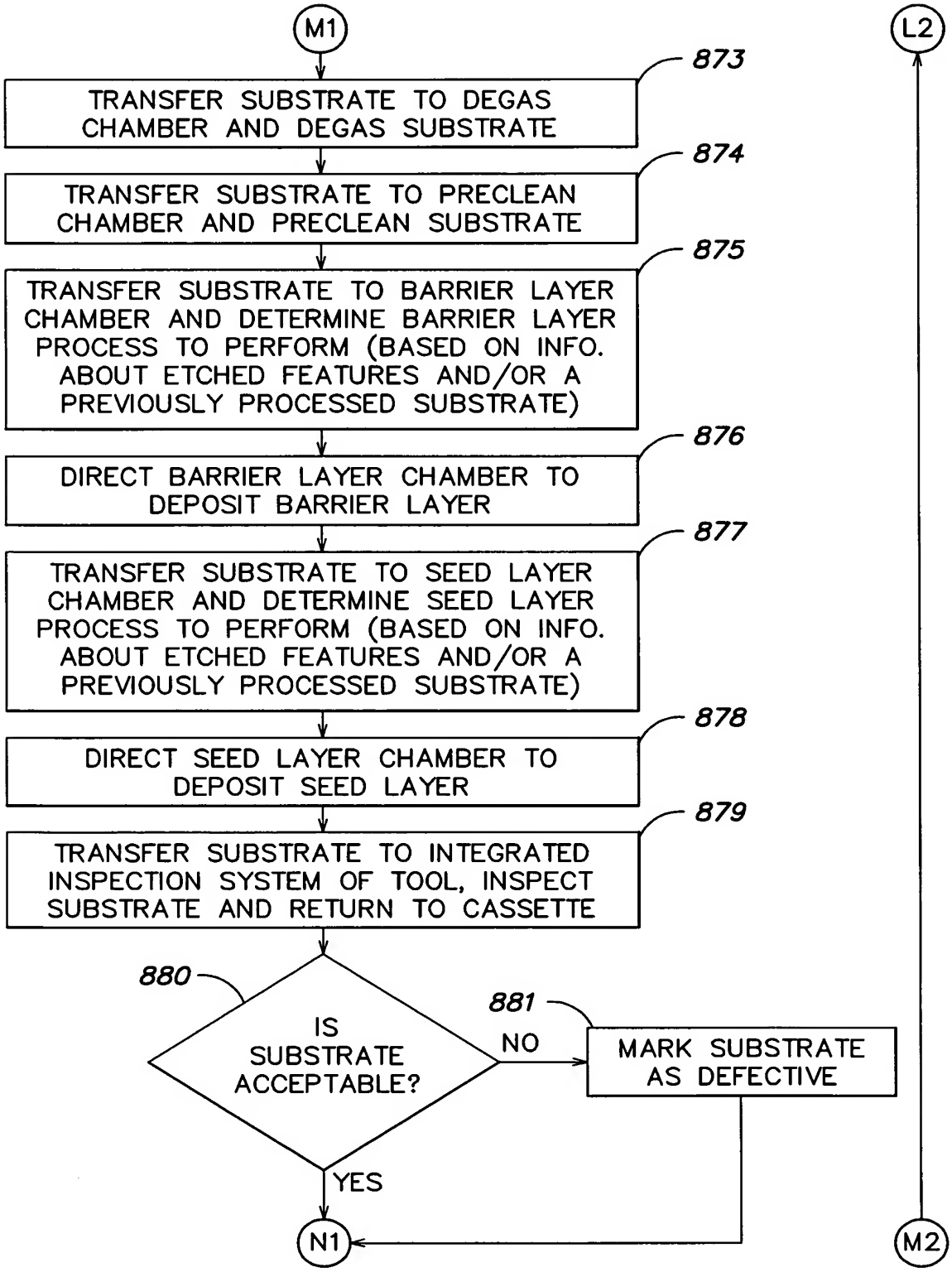
M1
L2
873
TRANSFER SUBSTRATE TO DEGAS CHAMBER AND DEGAS SUBSTRATE
874
TRANSFER SUBSTRATE TO PRECLEAN CHAMBER AND PRECLEAN SUBSTRATE
875
TRANSFER SUBSTRATE TO BARRIER LAYER CHAMBER AND DETERMINE BARRIER LAYER PROCESS TO PERFORM (BASED ON INFO. ABOUT ETCHED FEATURES AND/OR A PREVIOUSLY PROCESSED SUBSTRATE)
876
DIRECT BARRIER LAYER CHAMBER TO DEPOSIT BARRIER LAYER
877
TRANSFER SUBSTRATE TO SEED LAYER CHAMBER AND DETERMINE SEED LAYER PROCESS TO PERFORM (BASED ON INFO. ABOUT ETCHED FEATURES AND/OR A PREVIOUSLY PROCESSED SUBSTRATE)
878
DIRECT SEED LAYER CHAMBER TO DEPOSIT SEED LAYER
879
TRANSFER SUBSTRATE TO INTEGRATED INSPECTION SYSTEM OF TOOL, INSPECT SUBSTRATE AND RETURN TO CASSETTE
880
IS SUBSTRATE ACCEPTABLE?
881
NO
MARK SUBSTRATE AS DEFECTIVE
YES
N1
M2

FIG. 8M

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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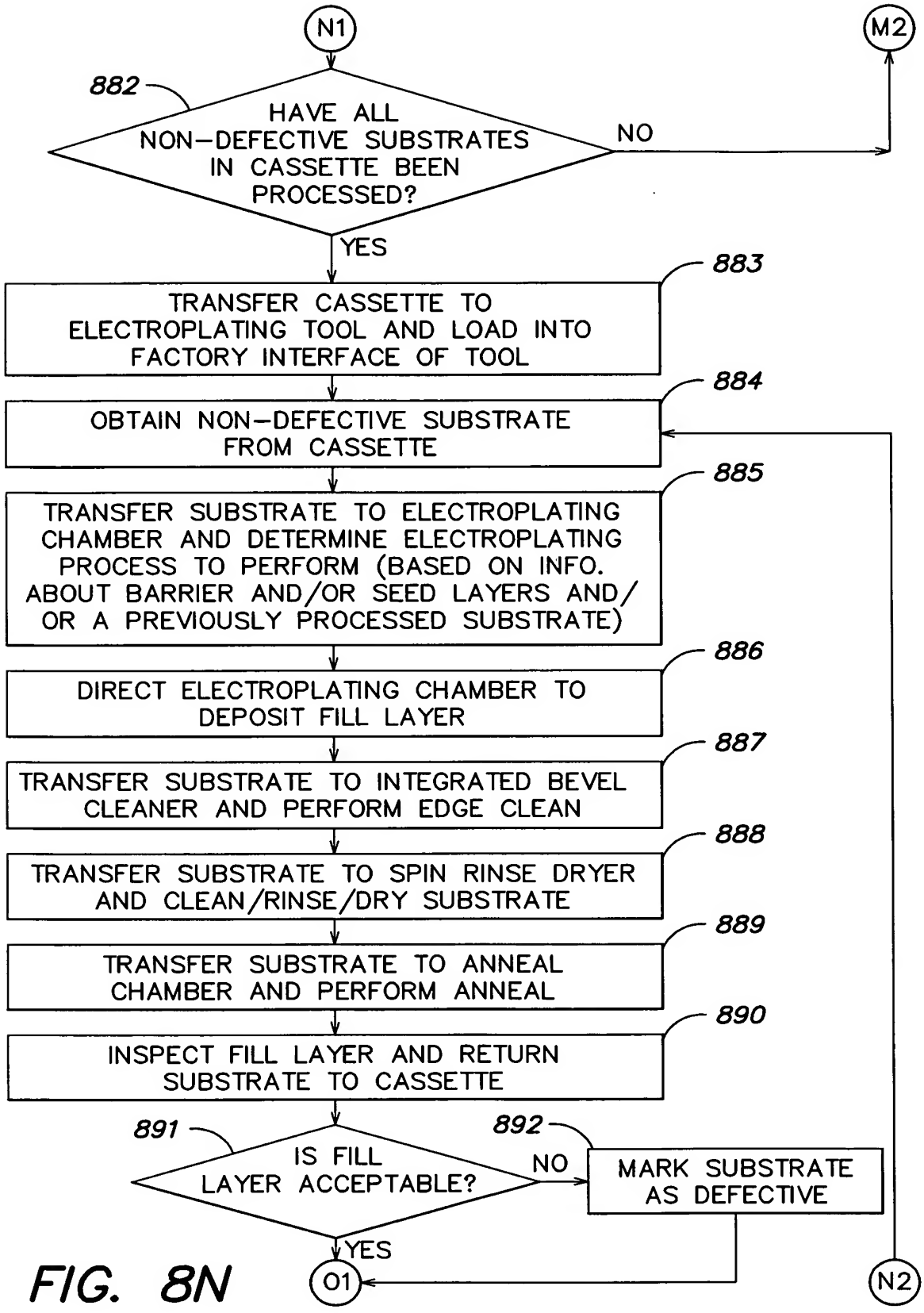
N1
M2
882
HAVE ALL NON-DEFECTIVE SUBSTRATES IN CASSETTE BEEN PROCESSED?
NO
YES
883
TRANSFER CASSETTE TO ELECTROPLATING TOOL AND LOAD INTO FACTORY INTERFACE OF TOOL
884
OBTAIN NON-DEFECTIVE SUBSTRATE FROM CASSETTE
885
TRANSFER SUBSTRATE TO ELECTROPLATING CHAMBER AND DETERMINE ELECTROPLATING PROCESS TO PERFORM (BASED ON INFO. ABOUT BARRIER AND/OR SEED LAYERS AND/OR A PREVIOUSLY PROCESSED SUBSTRATE)
886
DIRECT ELECTROPLATING CHAMBER TO DEPOSIT FILL LAYER
887
TRANSFER SUBSTRATE TO INTEGRATED BEVEL CLEANER AND PERFORM EDGE CLEAN
888
TRANSFER SUBSTRATE TO SPIN RINSE DRYER AND CLEAN/RINSE/DRY SUBSTRATE
889
TRANSFER SUBSTRATE TO ANNEAL CHAMBER AND PERFORM ANNEAL
890
INSPECT FILL LAYER AND RETURN SUBSTRATE TO CASSETTE
891
IS FILL LAYER ACCEPTABLE?
892
NO
MARK SUBSTRATE AS DEFECTIVE
YES
O1
N2

FIG. 8N

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
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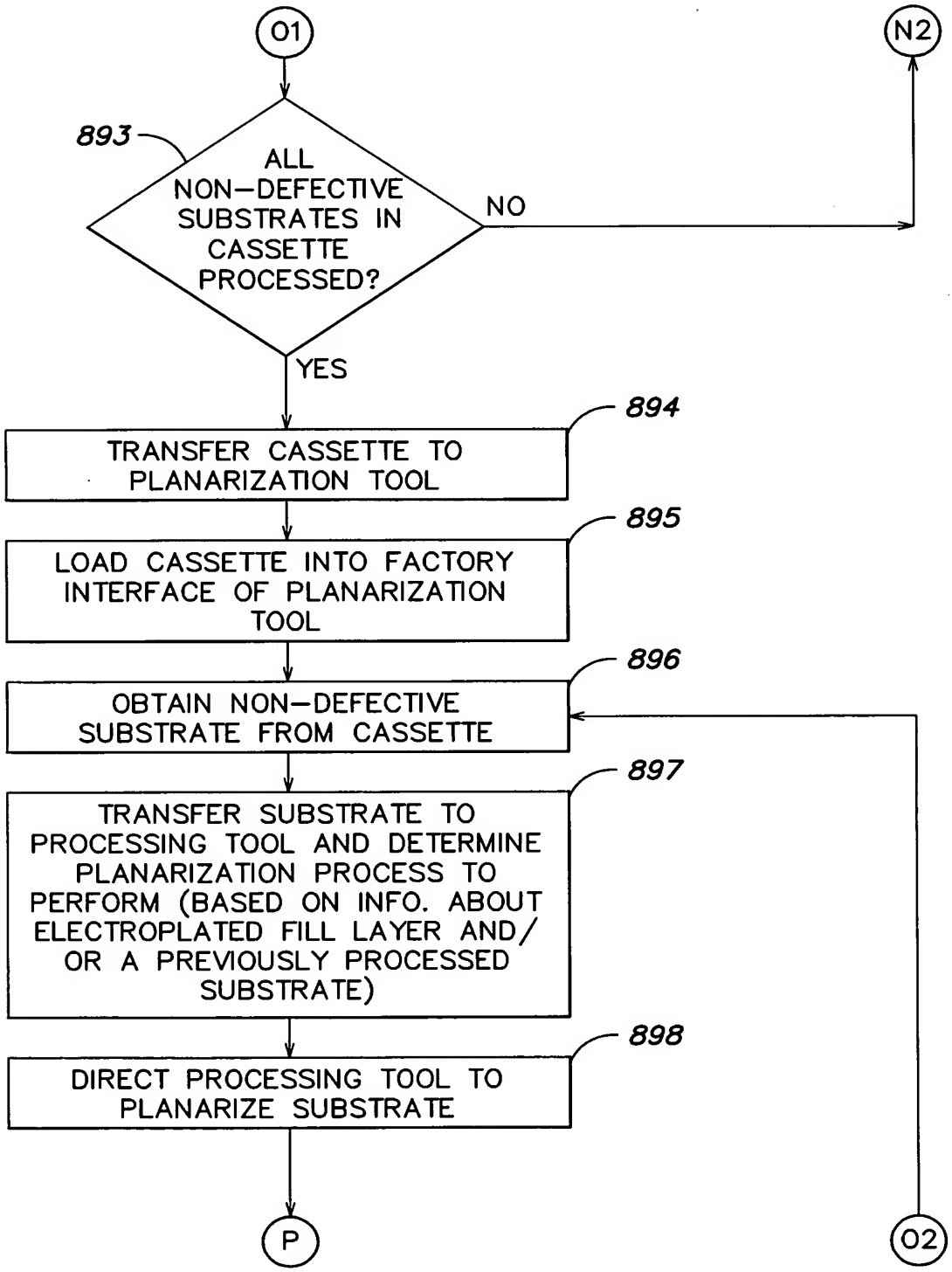
O1
N2
893
ALL NON-DEFECTIVE SUBSTRATES IN CASSETTE PROCESSED?
NO
YES
894
TRANSFER CASSETTE TO PLANARIZATION TOOL
895
LOAD CASSETTE INTO FACTORY INTERFACE OF PLANARIZATION TOOL
896
OBTAIN NON-DEFECTIVE SUBSTRATE FROM CASSETTE
897
TRANSFER SUBSTRATE TO PROCESSING TOOL AND DETERMINE PLANARIZATION PROCESS TO PERFORM (BASED ON INFO. ABOUT ELECTROPLATED FILL LAYER AND/ OR A PREVIOUSLY PROCESSED SUBSTRATE)
898
DIRECT PROCESSING TOOL TO PLANARIZE SUBSTRATE
P
O2

FIG. 80

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
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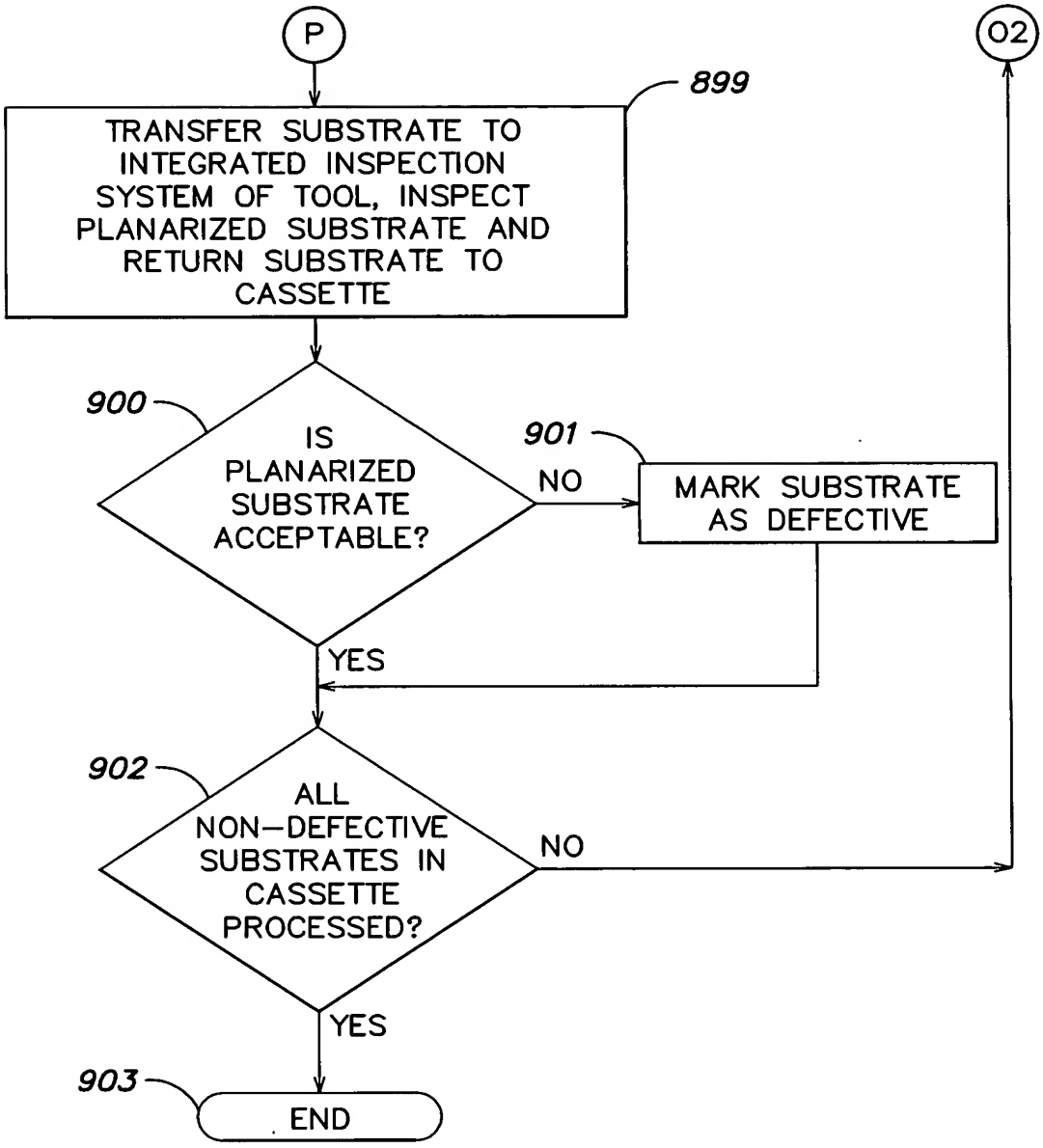
P
899
TRANSFER SUBSTRATE TO INTEGRATED INSPECTION SYSTEM OF TOOL, INSPECT PLANARIZED SUBSTRATE AND RETURN SUBSTRATE TO CASSETTE
900
IS PLANARIZED SUBSTRATE ACCEPTABLE?
901
NO
MARK SUBSTRATE AS DEFECTIVE
YES
902
ALL NON-DEFECTIVE SUBSTRATES IN CASSETTE PROCESSED?
NO
YES
903
END
02

FIG. 8P

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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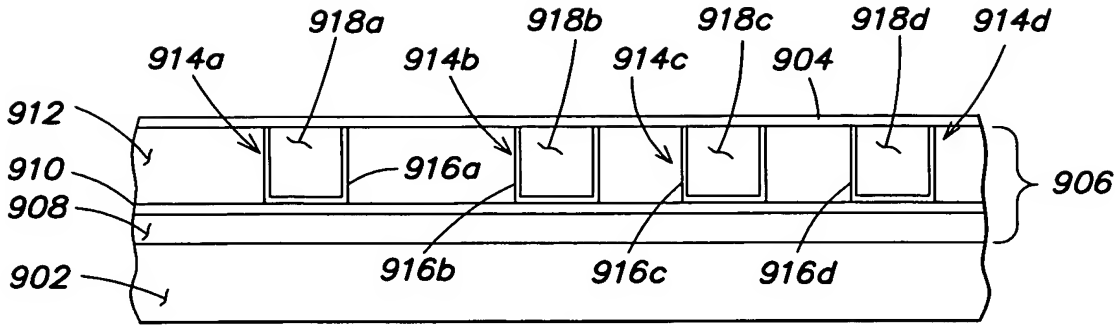

FIG. 9A

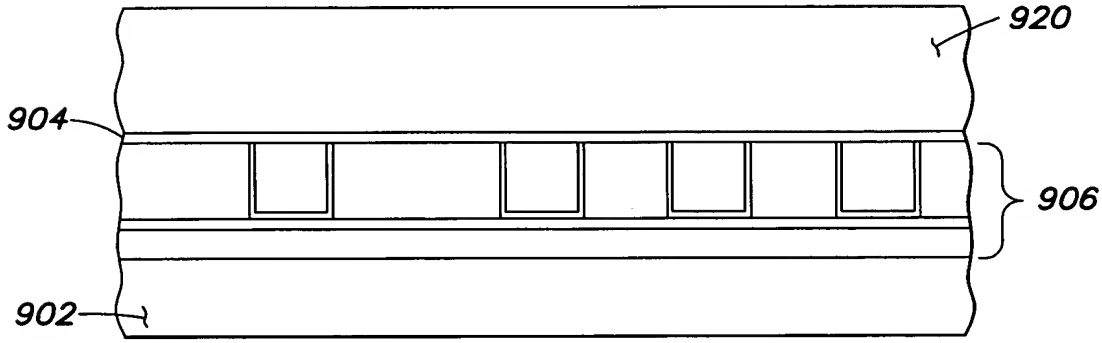

FIG. 9B

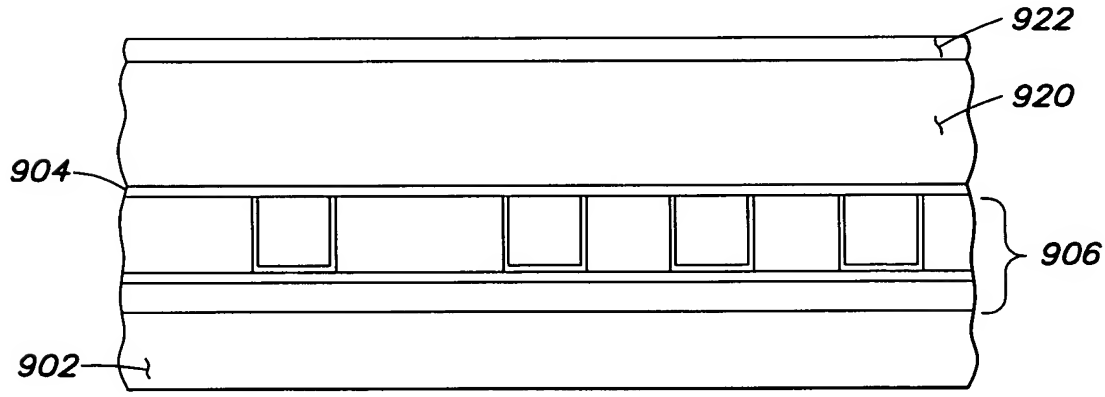

FIG. 9C

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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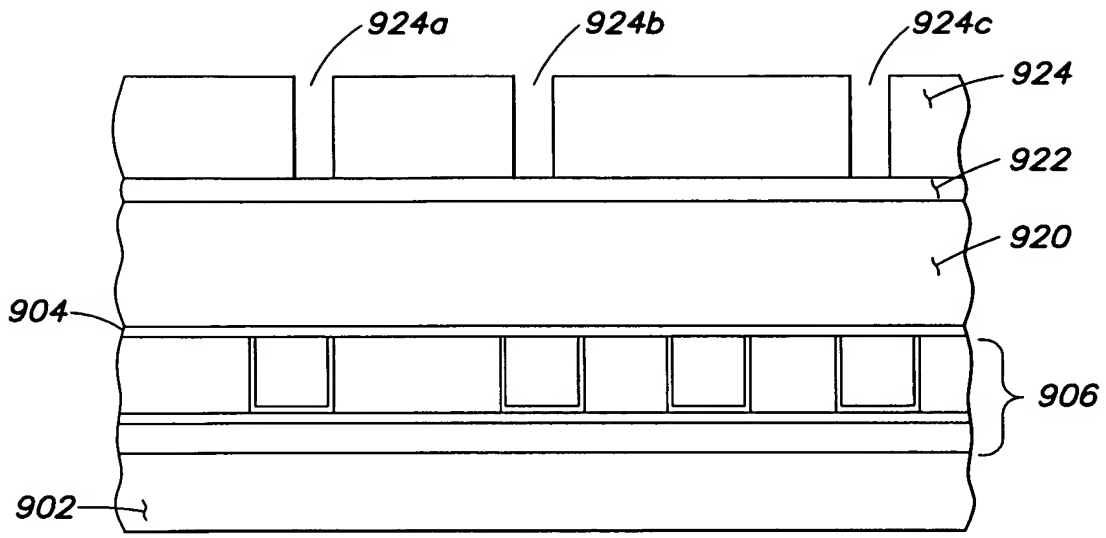
924a
924b
924c
924
922
920
904
906
902

FIG. 9D

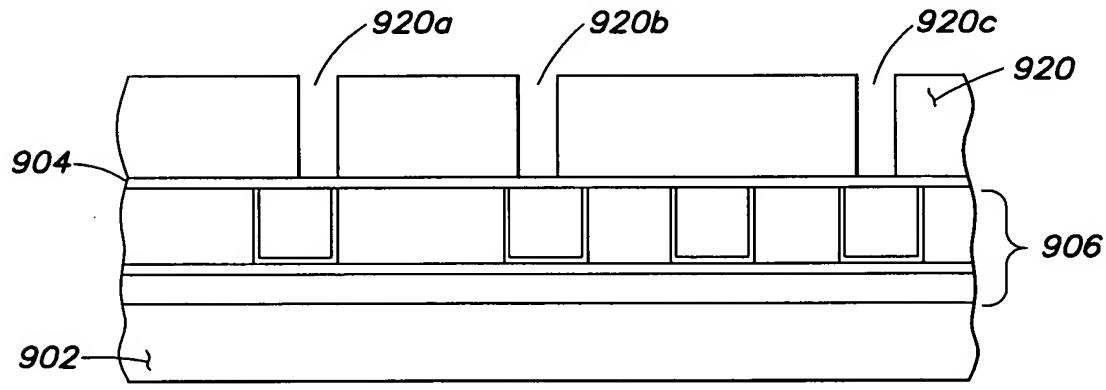
920a
920b
920c
920
904
906
902

FIG. 9E

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
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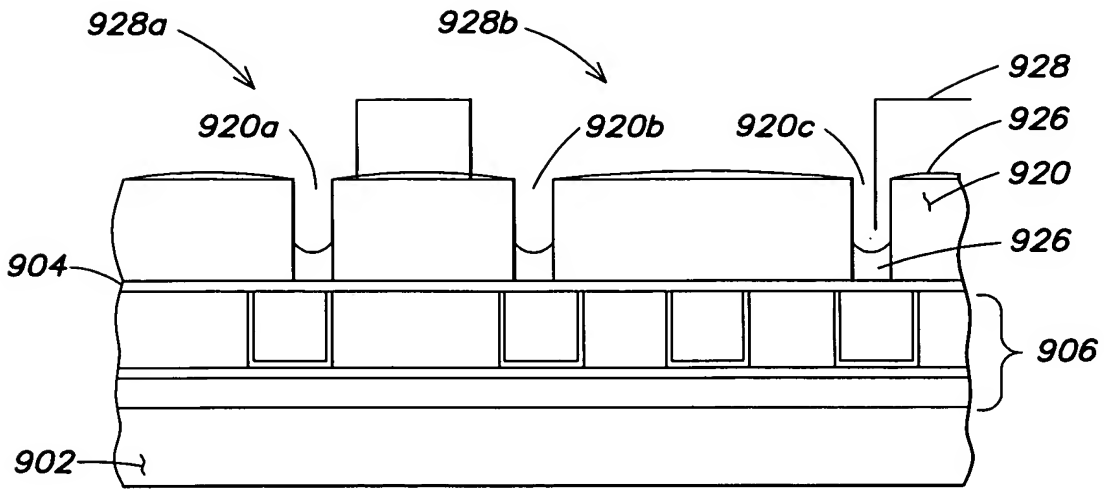
928a
928b
928
920a
920b
920c
926
920
926
904
906
902

FIG. 9F

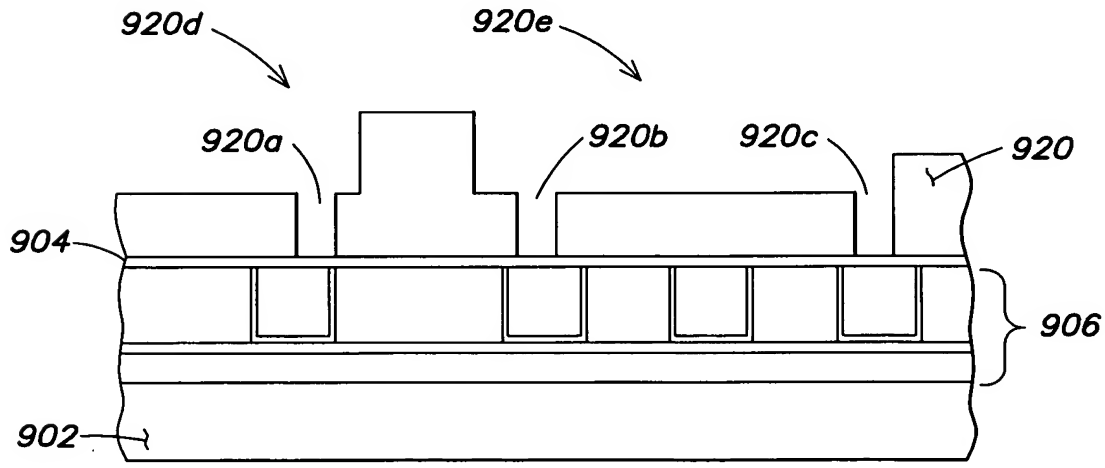
920d
920e
920a
920b
920c
920
904
906
902

FIG. 9G

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
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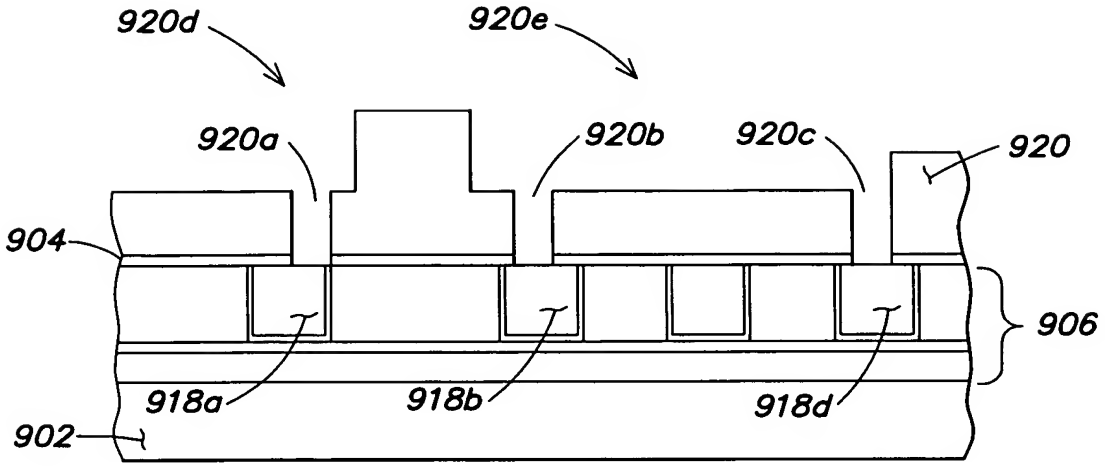
920d
920e
920a
920b
920c
920
904
906
918a
918b
918d
902

FIG. 9H

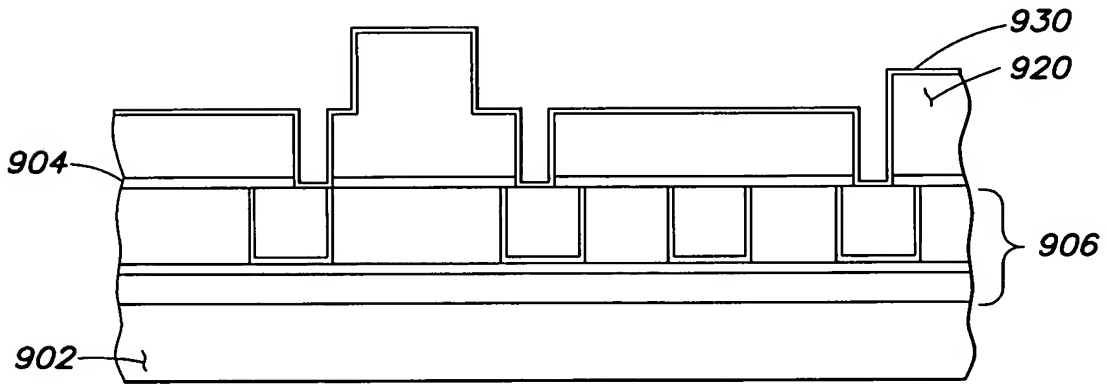
930
920
904
906
902

FIG. 9I

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
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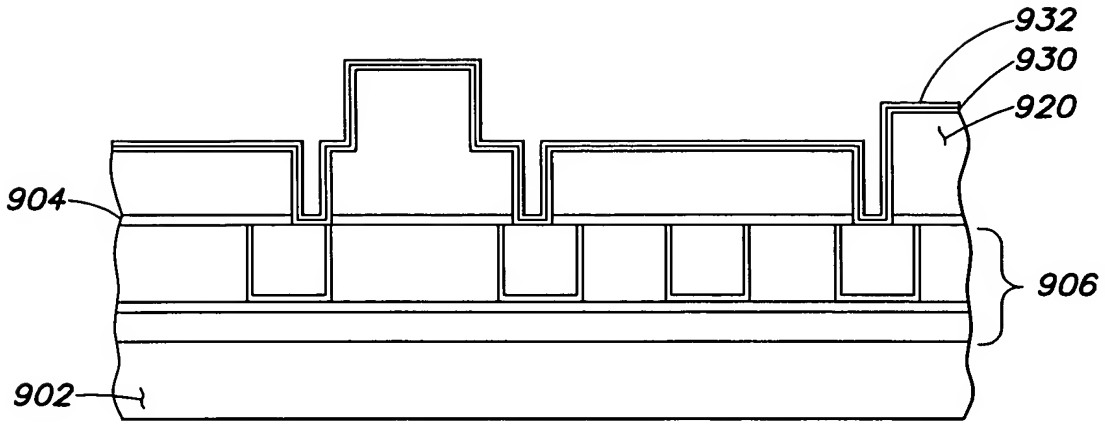

FIG. 9J

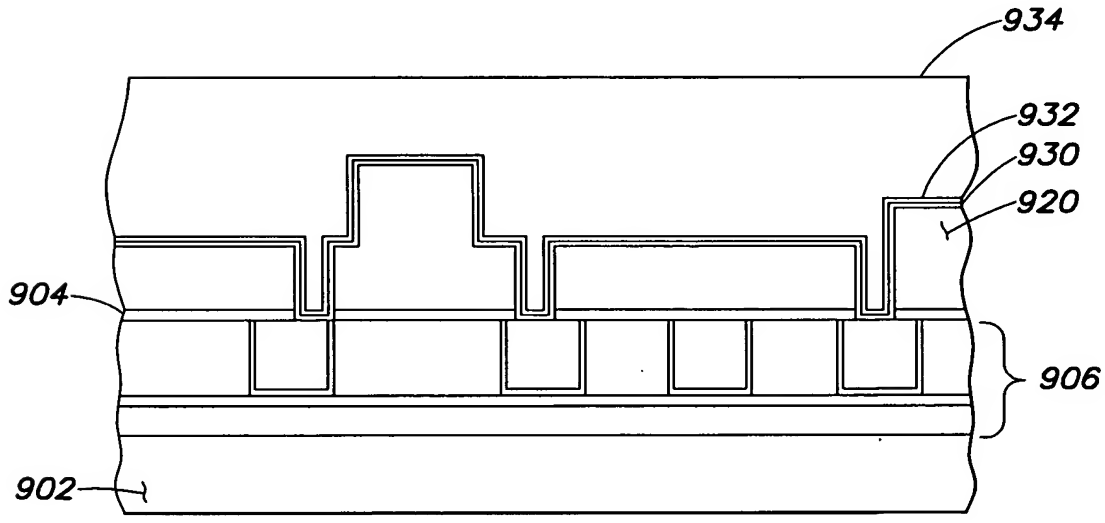

FIG. 9K

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
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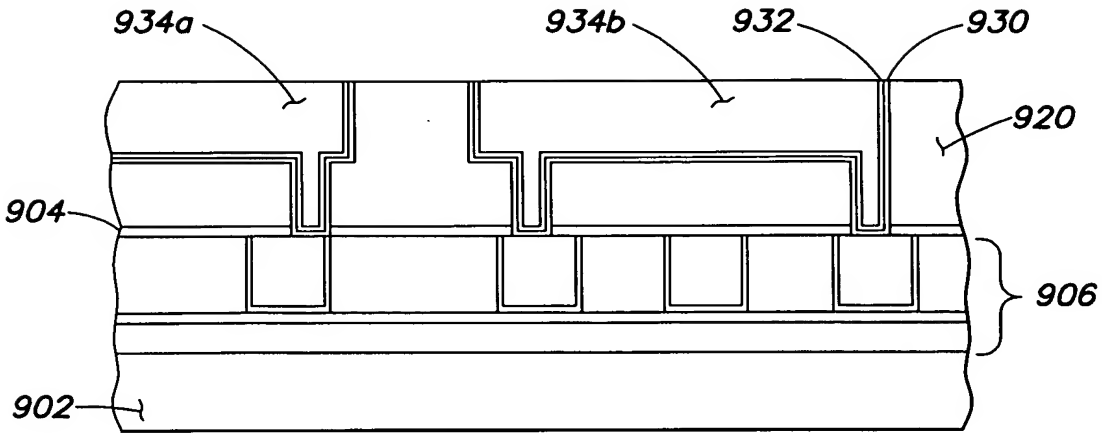

FIG. 9L

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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PROCESS ADJUSTED	BASIS FOR ADJUSTMENT	PROCESS PARAMETERS ADJUSTED	AFFECT OF ADJUSTMENT
Deposition within low K dielectric deposition tool 102	Feedforward information about interconnect features to be formed (e.g., density, dimensions, profile, etc.)	Chamber base pressure, processing pressure, processing temperature, processing time, processing power, gas flow rates, gas flow ratios, deposition time	Alters thickness, dielectric constant, stress level, refractive index, defect density and/or uniformity of deposited low K dielectric
Deposition within low K dielectric deposition tool 102	Feedback information about previously deposited low K dielectric (e.g., thickness, dielectric constant, stress level, index of refraction, uniformity, etc.)	Chamber base pressure, processing pressure, processing temperature, processing time, processing power, gas flow rates, gas flow ratios, deposition time	Alters thickness, dielectric constant, stress level, refractive index, defect density and/or uniformity of deposited low K dielectric
Clean within low K dielectric deposition tool 102	Feedback information about measured defect density following deposition	1. Clean time or frequency of cleaning;	1. Alters clean time or frequency of cleaning (to maintain desired defect density – e.g., increase one or both to reduce defect density);
		2. Season time;	2. Alters season time (to maintain desired defect density – increase to reduce defect density);

FIG. 10A

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PROCESS ADJUSTED	BASIS FOR ADJUSTMENT	PROCESS PARAMETERS ADJUSTED	AFFECT OF ADJUSTMENT
Etching within etch tool 106	Feedforward information about patterned masking layer (e.g., pattern density, feature dimensions, feature profile, etc.)	1. Select previously optimized process recipe based on pattern density;	1. Adjusts process based on selected process recipe, actual pattern density and desired etch results;
		Chamber base pressure, processing pressure, etch time, source power, substrate bias power, gas flow rates, gas flow ratios, deposition time, magnetic field strength	Adjusts etched feature depth, width and/or profile, uniformity, etc.
Etching within etch tool 106	Feedback information about previously etched features (e.g., dimensions or profile)	Chamber base pressure, processing pressure, etch time, source power, substrate bias power, gas flow rates, gas flow ratios, deposition time, magnetic field strength	Adjusts etched feature depth, width and/or profile, uniformity, etc.

FIG. 10B(1)
FIG. 10B(2)

FIG. 10B(1)

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
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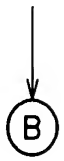

Clean within etch tool 106	Feedback information about previously measured defect density following etching	1. Chamber clean time or frequency of cleaning or season time;	1. Alters clean time or frequency of cleaning or season time (to maintain desired defect density – e.g., increase one or more to reduce defect density);
		2. O_2 flow;	2. Alters O_2 flow rate (e.g., increase O_2 flow to increase polymeric residue removal)
		3. Source power;	3. Alters source power (e.g., increase source power to remove residue faster);

FIG. 10B(2)

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
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PROCESS ADJUSTED	BASIS FOR ADJUSTMENT	PROCESS PARAMETERS ADJUSTED	AFFECT OF ADJUSTMENT
Barrier Layer Deposition Within Tool 112	Feedforward Information About Etched Features (e.g., Via and/or Line Dimensions)	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.
Barrier Layer Deposition Within Tool 112	Feedback Information About Previously Deposited Barrier Layer (e.g., Layer Thickness)	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.
Barrier Layer Deposition Within Tool 112	Feedback Information About Previously Measured Defect Density Following Barrier Layer Deposition	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.
Seed Layer Deposition Within Tool 112	Feedforward Information About Etched Features (e.g., Via and/or Line Dimensions)	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.
Seed Layer Deposition Within Tool 112	Feedback Information About Previously Deposited Seed Layer (e.g., Layer Thickness)	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.
Seed Layer Deposition Within Tool 112	Feedback Information About Previously Measured Defect Density Following Seed Layer Deposition	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.

FIG. 10C

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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(914) 332-9081

PROCESS ADJUSTED	BASIS FOR ADJUSTMENT	PROCESS PARAMETERS ADJUSTED	AFFECT OF ADJUSTMENT
Electroplating Within Tool 114	Feedforward Information About Barrier Layer (From Tool 112)	A), B) and/or C) Below	Alters Thickness, Rs, Uniformity, Reflectivity, Gap Fill, Defects, Backside Contamination. For Blanket as Well as Patterned Areas.
Electroplating Within Tool 114	Feedforward Information About Seed Layer (From Tool 112)	A), B) and/or C) Below	Alters Thickness, Rs, Uniformity, Reflectivity, Gap Fill, Defects, Backside Contamination. For Blanket as Well as Patterned Areas.
Electroplating Within Tool 114	Feedback Information About Previously Electroplated Fill Layer (e.g., Layer Thickness)	A), B) and/or C) Below	Alters Thickness, Rs, Uniformity, Reflectivity, Gap Fill, Defects, Backside Contamination. For Blanket as Well as Patterned Areas.
Electroplating Within Tool 114	Feedback Information About Previously Measured Defect Density Following Electroplating	A), B) and/or C) Below	Alters Thickness, Rs, Uniformity, Reflectivity, Gap Fill, Defects, Backside Contamination. For Blanket as Well as Patterned Areas.

A) ECP Plating Process: Flow Rate; Z–Height; Rotation Rate; Plating Recipe (e.g., Current and/or Voltage); Immersion Rotation Rate; Anode Amp–Hr; and/or Contact Ring Amp–Hr

B) Electrolyte/Bath Process: Temperature; Chemistry; Chemical Acidity; and/or Flow Rate

C) Anneal Process: Temperature Uniformity; Gas Flow Rates; and/or Pressure Before, During or After Anneal

FIG. 10D

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
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PROCESS ADJUSTED	BASIS FOR ADJUSTMENT	PROCESS PARAMETERS ADJUSTED	AFFECT OF ADJUSTMENT
Planarization within tool 116	Feedforward information about electroplated fill layer (from tool 114)	Retaining ring pressure; Membrane or inner tube pressure; slurry or rinsing fluid flow rate; head pressure or velocity; slurry rate/type/ concentration; polish/rinse /dry/cleaning time; substrate rotation rate.	Alters thickness, profile, Rs, uniformity. For blanket as well as patterned areas.
Planarization within tool 116	Feedback information about previously planarized surface (e.g., surface planarity)	Retaining ring pressure; Membrane or inner tube pressure; slurry or rinsing fluid flow rate; head pressure or velocity; slurry rate/type/ concentration; polish/rinse /dry/cleaning time; substrate rotation rate.	Alters thickness, profile, Rs, uniformity. For blanket as well as patterned areas.
Planarization within tool 116	Feedback information about previously measured defect density following planarization	Retaining ring pressure; Membrane or inner tube pressure; slurry or rinsing fluid flow rate; head pressure or velocity; slurry rate/type/ concentration; polish/rinse /dry/cleaning time; substrate rotation rate.	Alters thickness, profile, Rs, uniformity. For blanket as well as patterned areas.

FIG. 10E

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
Filing Date: January 16, 2004

Express Mail Label No.: EV605116109US

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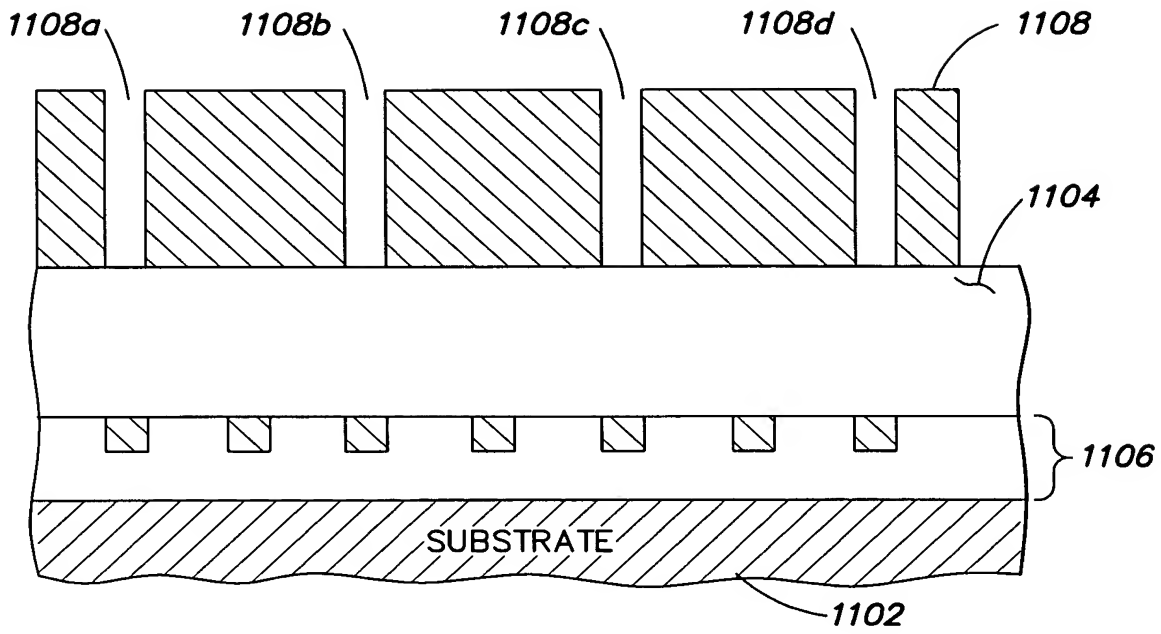

FIG. 11

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
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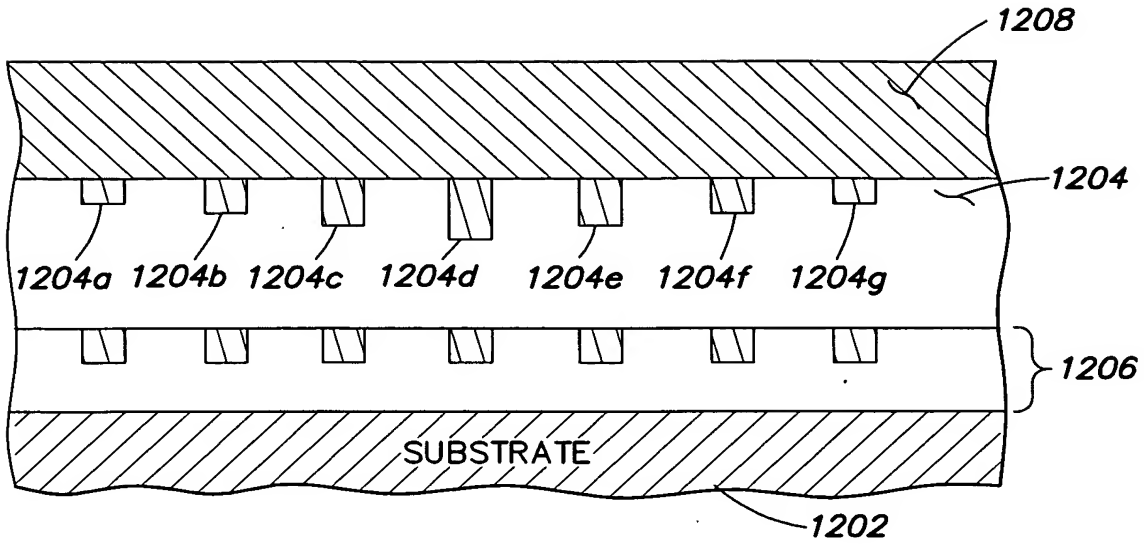

FIG. 12A

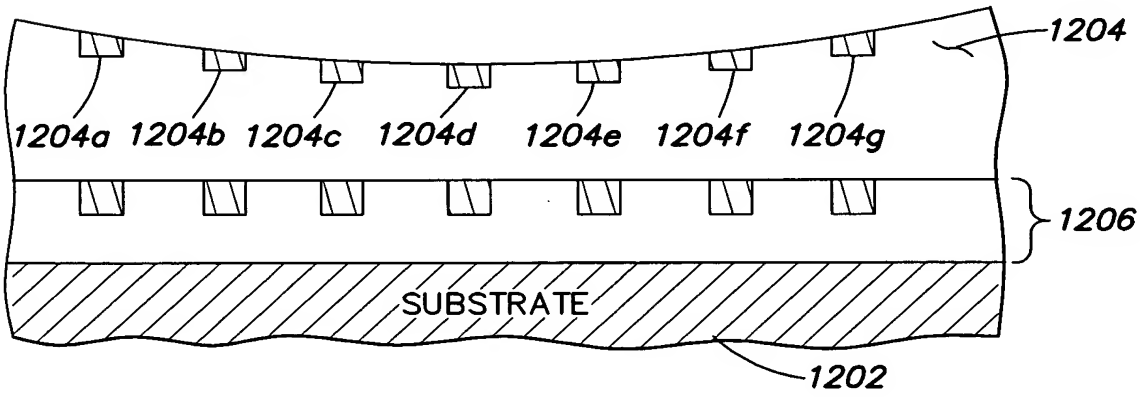

FIG. 12B

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
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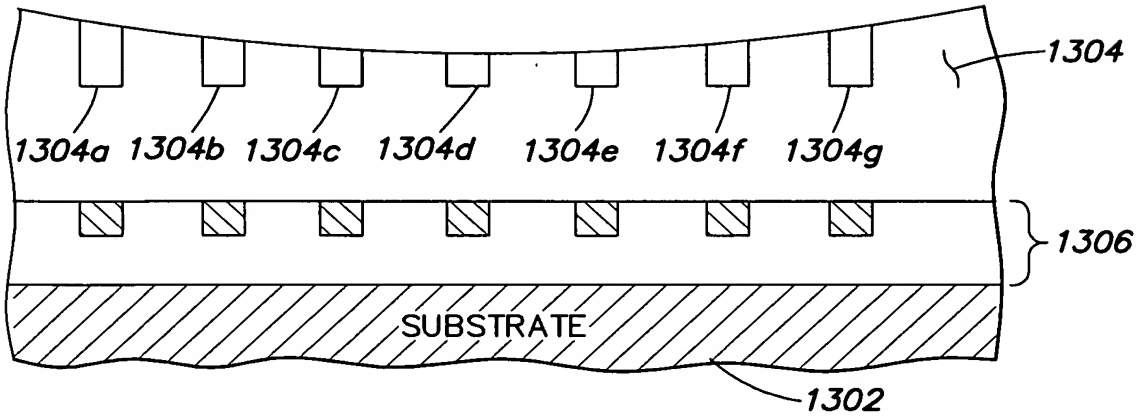

FIG. 13A

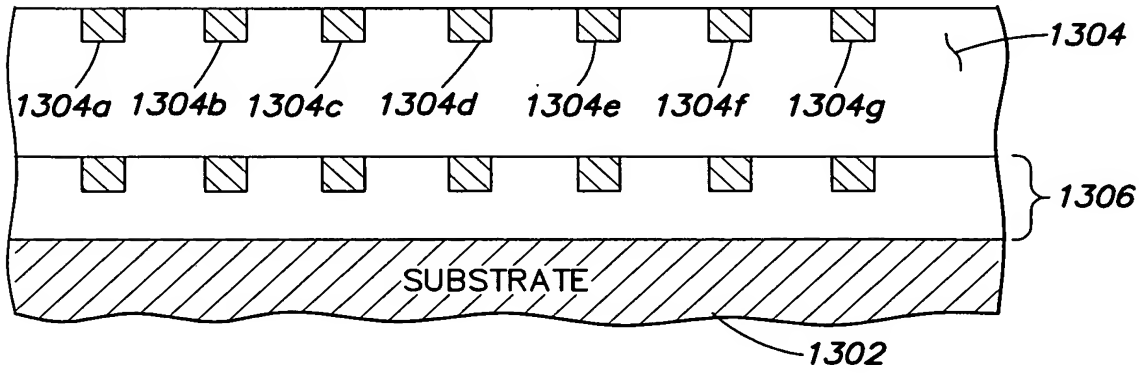

FIG. 13b

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
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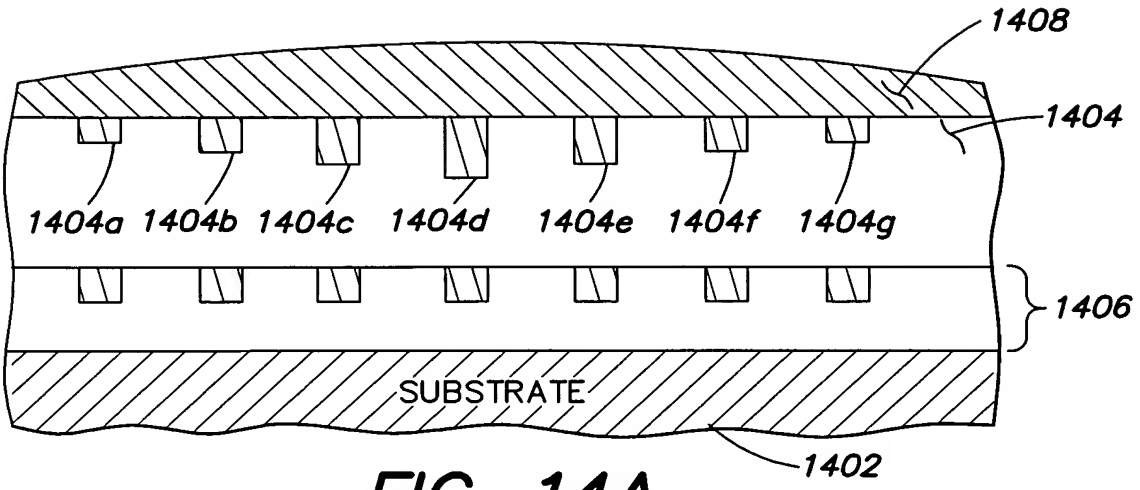

FIG. 14A

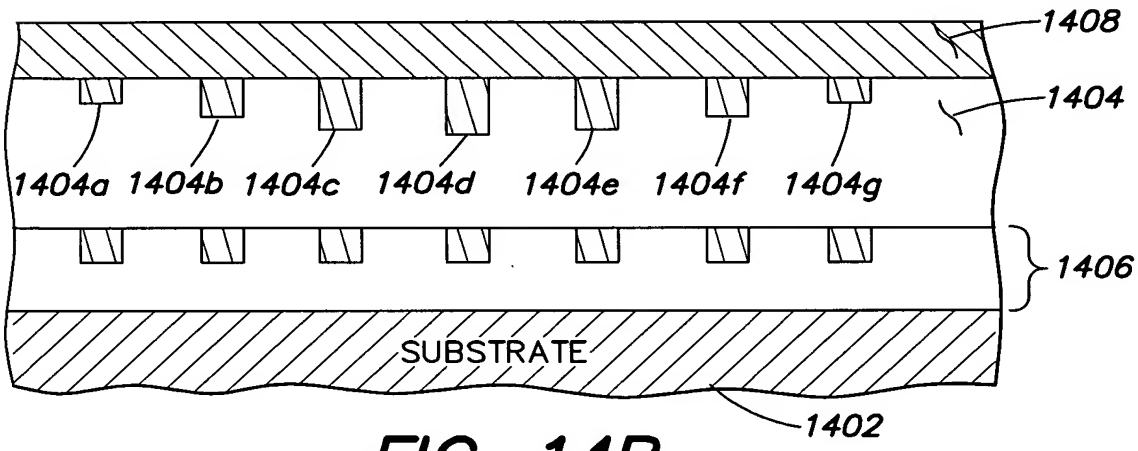

FIG. 14B

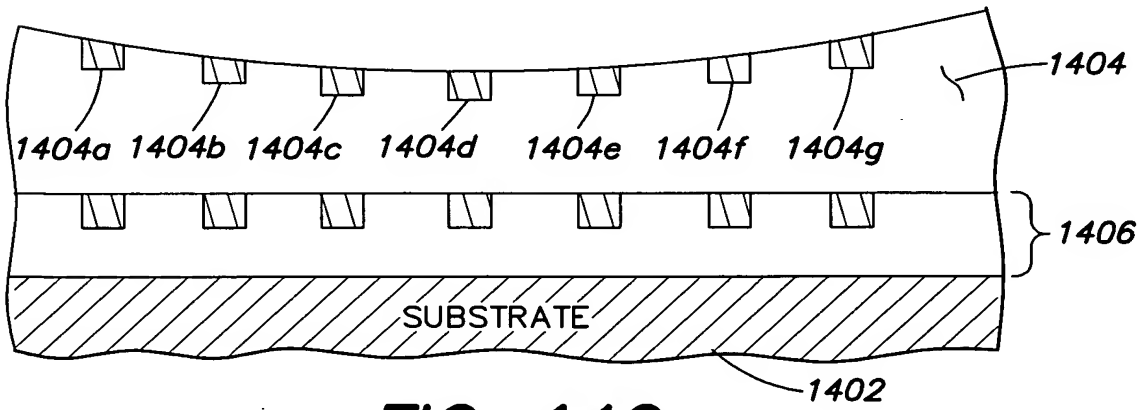

FIG. 14C

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and Michael D. Armacost
Serial No.: 10/759,801
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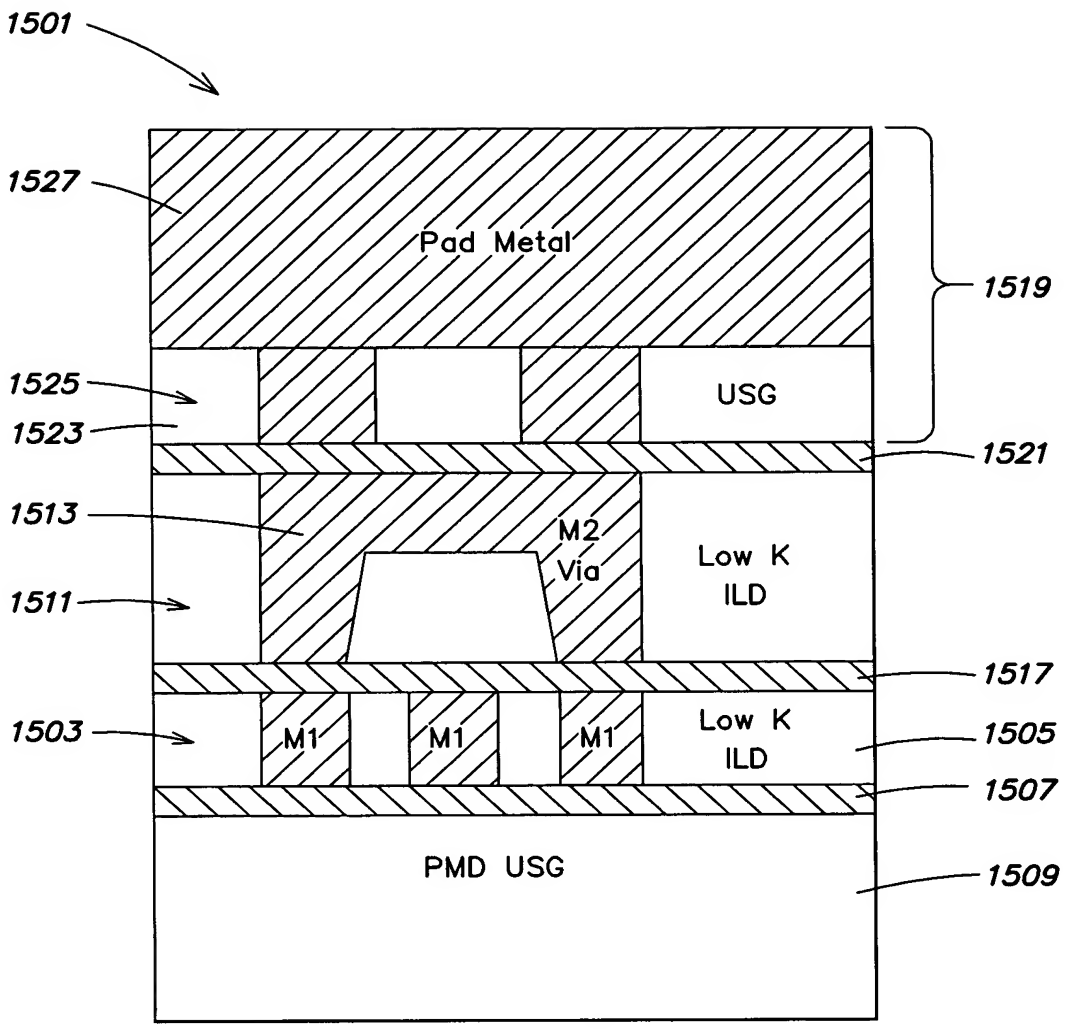
1501
1527
Pad Metal
1519
1525
USG
1523
1521
1513
M2
Via
Low K
ILD
1511
1517
1503
M1
M1
M1
Low K
ILD
1505
1507
PMD USG
1509

FIG. 15

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
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